The Mixed-Mode Reliability Stress of Silicon-Germanium Heterojunction Bipolar Transistors

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The Mixed-Mode Reliability Stress of Silicon-Germanium Heterojunction Bipolar Transistors

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I dedicate this thesis to my parents, Yaoquan Zhu and Guixia Chen, for their constant support throughout my life. I also dedicate this thesis to my wife, Tianwen Gu, and my sons, Robert and Alex.

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SUMMARY

The objective of the dissertation is to combine the recent Mixed-Mode reliability stress studies in silicon-germanium (SiGe) heterojunction bipolar transistors (HBTs). The thesis starts with a review of SiGe HBT fundamentals, development trends, and the conventional reliability stress paths used in industry, following which the new stress path, Mixed-Mode stress, is introduced. Chapter 2 is devoted to an in-depth discussion of damage mechanisms that includes the impact ionization effect and the self-heating effect. Chapter 3 goes onto the impact ionization effect using two-dimensional calibrated MEDICI simulations. Chapter 4 assesses the reliability of SiGe HBTs in extreme temperature environments by way of comprehensive experiments and MEDICI simulations. A comparison of the device lifetimes for reverse-EB stress and mixed-mode stress indicates different damage mechanisms govern these phenomena. The thesis concludes with a summary of the project and suggestions for future research in chapter 5.

This dissertation covers the following topics:

1. Introduces a new mixed-mode stress technique: time cumulative stress (Chapter II, also published in [23] and [24]).

2. Identifies impact ionization effects in the stress damage (Chapter II, also published in [23] and [24]).

3. Investigates for the first time mixed-mode damage using TCAD simulations at both room temperature and cryogenic temperatures (Chapter III and IV, also published in [23][24][62]).

4. Analyzes for the first time impact of self-heating on mixed-mode stress response, and identifies a temperature triggered damage threshold (Chapter II, will be published in [25]).

5. Explains the geometrical scaling issues in mixed-mode stress and explores mixed-mode stress reliability scaling trends (Chapter II, will be published in [25]).

6. Assesses for the first time SiGe HBT reliability at cryogenic temperatures (Chapter VI, also published in [62]).

CHAPTER I

INTRODUCTION

Since the invention of transistor in 1947, there has been an unprecedented expansion of semiconductor industry. As reported by the Semiconductor Industry Association (SIA), worldwide sales of semiconductors reached a new record of $213 billion in 2004, a 28% increase over the $166.4 billion in 2003. For the first six months of 2005, global microchip sales totaled $109.0 billion, an increase of 6.5% over the first six months of 2004. Today, the electronics industry is among the largest industries in many nations. The importance of microelectronics for the economic and social development worldwide continues to grow.

The development of new semiconductor technology has also seen a tremendous and steady progress in the past 50 years, and many new types of transistors have joined the semiconductor family. One of these is the silicon-germanium (SiGe) heterojunction bipolar transistor (HBT). In the evolution of semiconductor technology new transistors have continued to reduce in size over time, providing higher circuit speeds, higher packing densities, and lower power consumption. Consequently, modern electronic systems are far more powerful, cheaper, and smaller than their predecessors.

1.1 SiGe HBTs

During the past several years SiGe HBT technology has entered the global semiconductor electronics market with a bang, quickly becoming one of the fastest growing sectors in the semiconductor industry. There are two main reasons for this boom in SiGe technology. One is that the performance characteristics of SiGe devices are ideal for a broad range of emerging applications. SiGe devices have high current gain, high speed, low noise and low power dissipation. The other reason, which is actually the biggest attraction of SiGe HBT technology, is that SiGe HBTs can be easily integrated with conventional digital silicon chips. This has been termed SiGe bipolar complementary metal-oxide semiconductor (SiGe BiCMOS) technology. The SiGe chip is not only

cheaper, but also naturally offers a better solution in emerging system-on-chip (SOC) and system-on-package (SOP) ICs than III-V compound transistors.

The outstanding performance of SiGe HBT, particularly in terms of current gain (β), early voltage (V_A), and cutoff frequency (f_T), can best be explained by examining a schematic energy bandgap diagram. The more the amount of Ge is introduced into Si, due to the difference in bandgaps of two elements, the smaller the bandgap of the resulting alloy is. The standard rule of thumb for SiGe device design is 74 meV/percent of Ge (mole fraction), which represents an acceptable approximation across the practical range of 0-30% Ge content used in transistor design [1]. Figures 1 and 2 illustrate a typical SiGe *npn* HBT with linearly graded base and constant doping in emitter, base and collector.

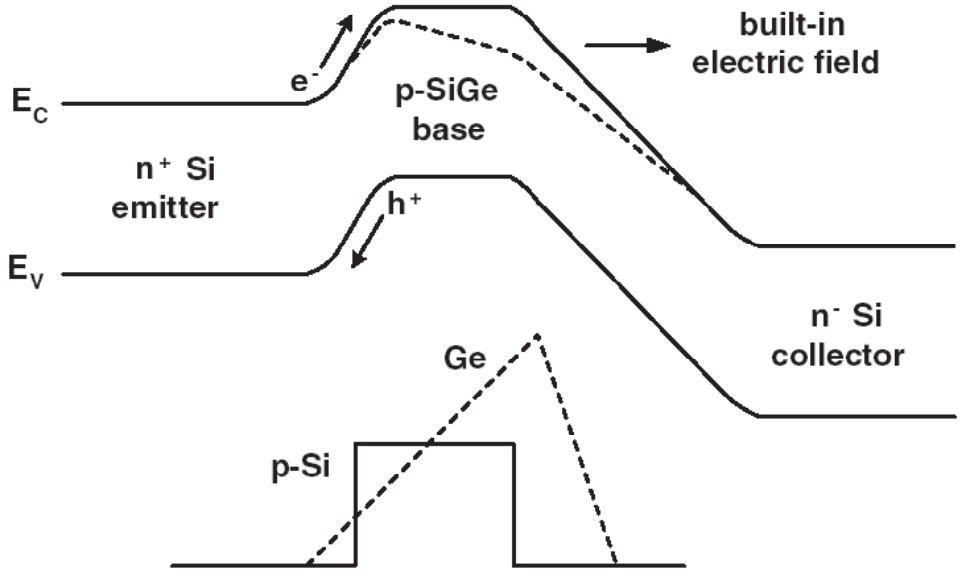

Figure 1: Energy band diagram for a Si BJT and graded-base SiGe HBT.

Here, E_{gb0} is the bandgap for Si material under low-doping, $\triangle E_{gb}^{app}$ is the bandgap narrowing induced by heavy doping, $\triangle E_{g,Ge}(x)$ is the Ge-induced bandgap offset at position x, and $\triangle E_{g,Ge}(grade)$ $= \triangle E_{g,Ge}(W_b) - \triangle E_{g,Ge}(0)$. With a lower potential barrier, the injection of electrons from the emitter into the base increases exponentially for the same applied V_{BE}. Thus, the collector current and current gain both increase while the base current remains unchanged. The current ratio between

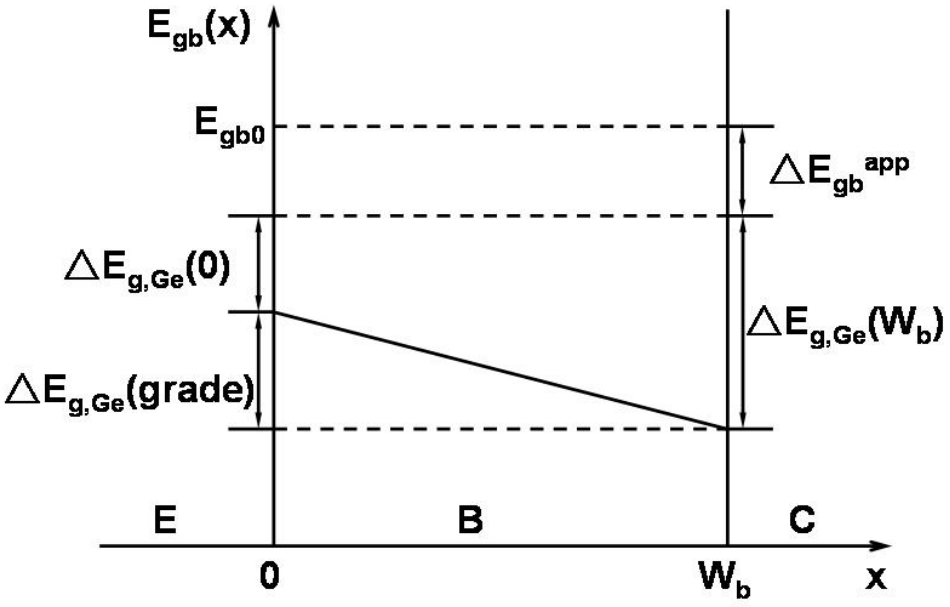

Figure 2: Schematic base bandgap in a SiGe HBT with a linearly graded Ge profile.

SiGe and Si is given by

$$\frac{\beta_{SiGe}}{\beta_{Si}}\Big|_{V_{BE}} \approx \frac{\gamma\eta\triangle E_{g,Ge}(grade)e^{\triangle E_{g,Ge}(0)/kT}}{kT\{1-e^{-\triangle E_{g,Ge}(grade)/kT}\}} \tag{1}$$

where γ is the effective density of states ratio between SiGe and Si, and η is the minority carrier diffusion ratio between SiGe and Si [1]. The early voltage V_A increases since the smaller base bandgap near the collector-base junction suppresses the neutral base depletion for increasing applied CB voltage. The V_A ratio between SiGe and Si is expressed by

$$\frac{V_{A,SiGe}}{V_{A,Si}}\Big|_{V_{BE}} \approx e^{\triangle E_{g,Ge}(grade)/kT}\{\frac{1-e^{-\triangle E_{g,Ge}(grade)/kT}}{\triangle E_{g,Ge}(grade)/kT}\} \tag{2}$$

The base transit time decreases since the graded energy bandgap could generate a "quasi-electric" field to accelerate charged carriers in the base. The base current is now composed by not only the diffusion current but also the drift current. Hence, a higher cut-off frequency (f_T) is achieved. The transit time ratio of τ_b is

$$\frac{\tau_{b,SiGe}}{\tau_{b,Si}} \approx \frac{2kT}{\eta\triangle E_{g,Ge}(grade)}\{1-\frac{kT\{1-e^{-\triangle E_{g,Ge}(grade)/kT}\}}{\triangle E_{g,Ge}(grade)}\} \tag{3}$$

1.2 SiGe HBT Performance Trends

Although SiGe technology is a new star in the semiconductor world, the concept of SiGe HBT is almost as old as the invention of the transistor itself. In the first transistor patent, Shockley mentioned combining Si and Ge to form a SiGe HBT. In 1957, Kroemer pioneered the theory of HBT [2]. However, the early HBTs were manufactured using III-V compound semiconductors, like gallium-arsenide (GaAs) and indium phosphide (InP), because effective heterojunction formation requires two semiconductors with similar lattice spacing. Unfortunately, Ge has a larger lattice constant than Si, with a lattice mismatch of roughly 4.2%. It was 30 years before the concept could be realized practically due to material growth limitations. Device-quality SiGe films were first achieved in the mid-1980s using ultra-high vacuum/chemical vapor deposition (UHV/CVD) techniques [3]. Once this obstacle was overcome, SiGe technology was ready to enter its golden age. Figures 3 and 4 show the representative cross-section and doping profile of the first-generation (50 GHz peak

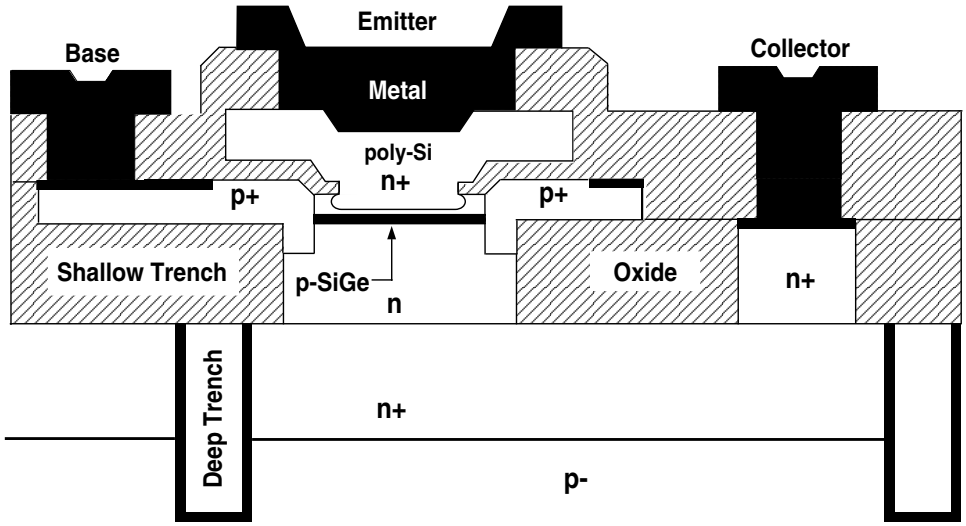

Figure 3: Representative cross-section of the first- and second-generation SiGe HBTs.

f_T) SiGe HBT demonstrated by IBM in 1990 [4]. The year 2001 was a milestone. During the first six months, the second-generation (120 GHz peak f_T) SiGe HBT was successfully fabricated [5], followed almost immediately, in November, by breaking the 200 GHz peak f_T barrier, thus introducing the third-generation SiGe HBT [6]. Today, the peak f_T of state-of-the-art SiGe HBTs is even higher, reportedly as high as 350 GHz [7]. Table 1 lists the representative parameters for three

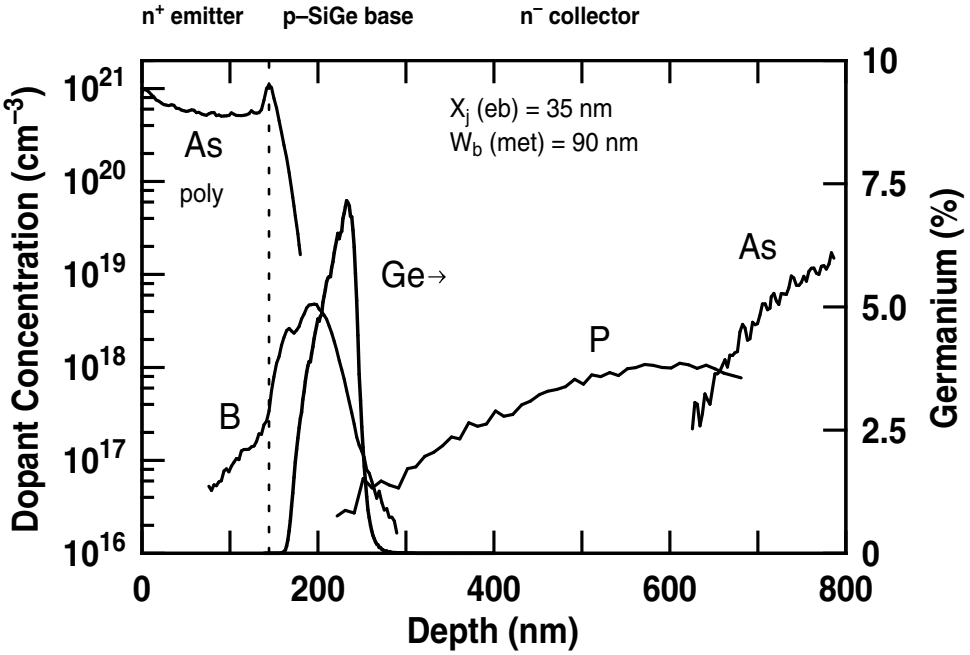

Figure 4: Representative doping profile of the first-generation SiGe HBT.

distinct SiGe HBT generations.

As SiGe HBT technology evolves, optimized lateral and vertical scaling is being used to obtain an improved frequency response. To suppress the Kirk effect and the heterojunction barrier effect, the collector doping has been increased. Thus, as shown in the Table 1, the collector current density (J_C) at the peak cutoff frequency (f_T) rises with scaling. However, the increased collector doping needed to sustain this performance gain unfortunately produces a strong increase in the collector-base junction electric field, which in turn increases impact ionization, raising concerns for device

Table 1: Representative parameters for three distinct IBM SiGe HBT BiCMOS technology generations (after [1]).

Parameter	First (5HP)	Second (7HP)	Third (8HP)
$W_{E,eff}$ (μm)	0.42	0.18	0.13
peak β	100	200	400
V_A (V)	65	120	>150
BV_{CEO} (V)	3.3	2.5	1.7
BV_{CBO} (V)	10.5	7.5	5.5
peak f_T (GHz)	47	120	207
peak f_{max} (GHz)	65	100	285

reliability.

The other potential reliability issue arises due to the self-heating effect. Several studies have reported measurements of the thermal resistance of SiGe HBTs [8]-[12]. The results show that thermal resistance increases as the transistor feature size scales down. This is due to the smaller cross-sectional area enclosed by a deep-trench, which effectively pinches the heat flux towards the substrates. For the same power input, the larger thermal resistance leads to severe junction temperatures. Thus, some device degradation mechanisms will be accelerated, and the device lifetime is likely to be shorter.

1.3 The Reliability Stress

The reliability of devices is one of the most critical issues in circuit and system design. The device must be proven to be both robust and reliable under typical circuit operating conditions. That is, the circuits and, most importantly, the systems constructed from those circuits, must not wear out or degrade to a level at which they will fail in the field over the functional life of the system [13].

How is the "reliability" of a transistor defined? Or, how is it possible to ensure the adequate reliability of a transistor? The answer is that one can subject devices to extreme operating conditions, known as "accelerated" conditions, for a given length of time. The "reliability" of the transistor is then defined in terms of the measured change in a given defined device metric after a given amount of time under stress (e.g. the stress time it takes to produce a decrease in current gain of 10%). From this time-dependent stress data, an extrapolated "lifetime" of the technology can be projected. If the projected lifetime greatly exceeds the intended system life of the part, then all is well and the device is considered to be reliable [13].

Given there are different damage mechanisms, research into reliability stress has historically proceeded along two paths in bipolar technology, namely high forward collector current density (J_C) stress [14]-[16] and the reverse-bias emitter-base (EB) junction stress [17]-[19].

Typically high forward J_C stress is examined under a large J_C near peak f_T at elevated temperatures (e.g. 140 °C). The excess base current leakage is generally attributed to the electromigration-induced pressure on the emitter contact, resulting in a decrease in collector current with increasing

stress time and consequently current gain degradation. Recently, Rieh *et al.* [20] demonstrated that much higher current levels, for example, 4 × J_C at peak f_T, damage devices much faster leading to projected lifetimes that were almost the same as those predicted by extrapolations of lower level current density stress.

Reverse EB stress is generally examined under high reverse EB bias at reduced temperatures (e.g. -40 °C). Here, the stress-induced hot electrons (or holes [18]) are injected into the EB spacer oxide, thereby introducing generation/recombination (G/R) center traps that lead to excess non-ideal base current and current gain degradation as well as increased low-frequency noise [21].

Recently, a new damage pattern induced by so-called "mixed-mode" stress was reported in [22] for the first-generation SiGe HBTs where a high voltage is applied to the collector-base junction at the same time as a high forward current is flowed through the device under test (DUT). Post-stress base current leakages were observed for both forward-mode Gummel and inverse-mode Gummel characteristics, indicating a new damage mechanism that is fundamentally different to the conventional stresses described above. Thus, several questions arise: What is the damage mechanism? Does the ambient temperature, including extreme temperature environments, affect the device reliability? How does the technology generation influence the device's reliability? These questions are important for device fabrication, device modeling and circuit design. Hence, the objective of this thesis is to address answer these questions and build a solid basis for future research.

CHAPTER II

MIXED-MODE RELIABILITY STRESS

As mentioned in the previous chapter, mixed-mode stress (MMS) leads to a fundamentally different damage pattern compared to reverse emitter-base stress and high forward current stress. In this chapter, the damage mechanism of MMS is explored using two newly developed stress techniques. The first technique is time cumulative stress, while the other is termed current sweep stress. After introducing both stress techniques, the comprehensive measured data will be discussed in detail for both the impact ionization and self-heating effects.

2.1 Stress Techniques

Previously, a less-than-optimum "aggressive Gummel" technique was used to stress 50 GHz SiGe HBT devices [22] where the forward-mode Gummel was measured under "aggressive" conditions, namely a high fixed V_{CB} (e.g. $V_{CB} = 3\ V$) and a high V_{BE}, which is swept (e.g. V_{BE}=1.3 V at room temperature). However, this technique has several disadvantages. First, when V_{BE} is swept from low to high, the collector current also increases. So the stress current varies during the MMS. Next, it is impossible to estimate the stress time accurately. When V_{BE} reaches the assigned value, the whole stress procedure stops immediately, and the exact stress time can't be controlled. As the total injected carrier number is the product of the stress current and the stress time, the exact total injected carrier number is unknown, and there is no way to conduct further quantitative studies.

An advanced MMS technique is implemented in this work. The new technique uses a robust, time-dependent stress setup [23] [24] to precisely control the injected charges. This is termed time cumulative stress. To produce MMS, a current source is pulled from the emitter, and simultaneously a reverse-biased voltage source is applied to the base-collector junction while the base is grounded. Transistors are then stressed with the assigned emitter current density J_E and collector-base voltage V_{CB} over a given time interval. Periodically interrupting the stress at selected time intervals makes it possible to execute necessary measurements, such as forward-mode and inverse-mode Gummel

measurements. Figure 5 compares both stress techniques based on the forward-mode Gummels. Obviously, the new methodology has taken the time cumulative effect into consideration.

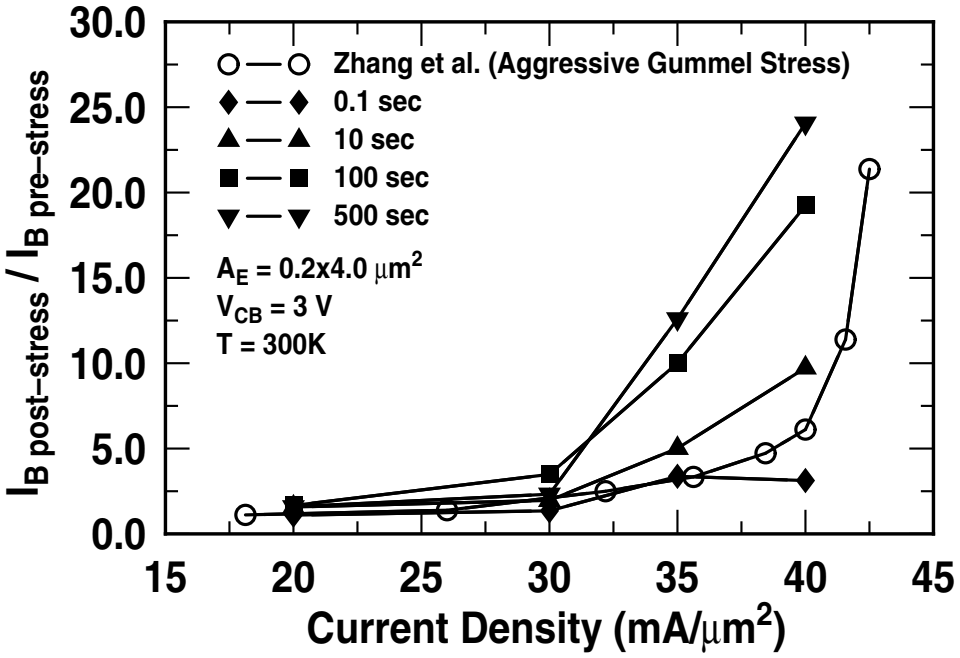

Figure 5: Base current damage ratio vs. current density comparing the "aggressive Gummel" stress technique [22] with the advanced stress technique.

Recently a new stress technique, current sweep stress, has been developed based on the second MMS technique by Cheng [25]. The difference is that here the stress current density increases from a very low initial current density until the device is no longer functional, while the stress time interval is fixed for each current density point. In this work, to obtain a better resolution, the stress current increases exponentially between 1 nA/μm^2 to 1 mA/μm^2 and linearly thereafter. At each stop, the forward-mode Gummel and inverse-mode Gummel are recorded. Finally, a damage spectrum, the plot of base current degradation (ratio) versus current density, can be constructed.

2.2 Impact Ionization Effect

At a sufficiently high electric field, an electron in the conduction band can gain enough energy to lift an electron from the valence band into the conduction band, generating a pair of a free "hot" electron and a free "hot" hole in the conduction band and valence band, respectively. This procedure is termed *impact ionization*. Obviously, the higher the electric field, the stronger the impact

ionization, the more hot carriers, and the more hot carrier-induced traps.

During MMS, strong impact ionization is expected due to the high voltage applied to the CB junction. In this section, comprehensive data are discussed for the impact ionization effect. All tests are based on the second-generation SiGe HBTs from a 0.18-μm commercial IBM SiGe HBT BiCMOS technology. The device has a planar, self-aligned structure, deep and shallow trench isolation, and a thermodynamically stable, UHV/CVD epitaxial graded SiGe base layer with a peak Ge content of about 25% [26]. A representative cross-section of the device is shown in Figure 3. Details of the fabrication process can be found in [5].

2.2.1 *dc* Degradation

Figures 6 and 7 represent typical forward-mode and inverse-mode Gummel characteristics after a mixed-mode stress test with $J_E = 40$ mA/μm^2 and $V_{CB} = 3.0$ V. It is clear that the base leakage

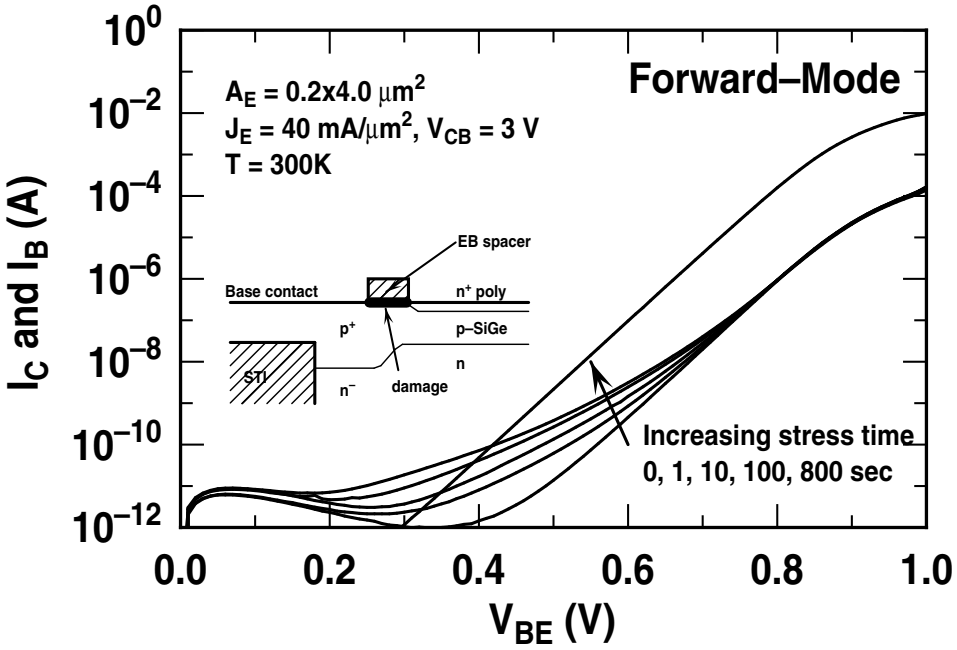

Figure 6: Forward-mode Gummel characteristics showing the base current degradation with increasing stress time.

current shifts up (degrading the current gain β) when the time under stress increases, while I_C is unchanged. The base current degradation is a function of cumulative stress time. As expected, MMS creates interface traps and subsequent generation/recombination (G/R) base current leakage at both

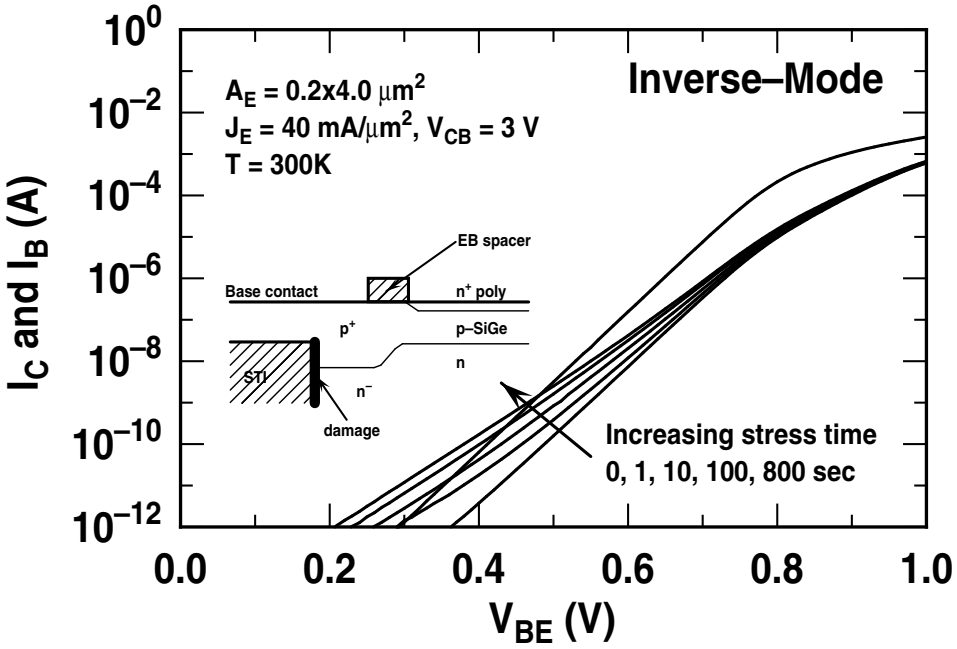

Figure 7: Inverse-mode Gummel characteristics showing the base current degradation with increasing stress time.

the emitter-base spacer (forward-mode, Figure 6) and at the STI edge (inverse-mode, Figure 7). The Shockley-Read-Hall (SRH) process dominates the recombination at room temperature, since the ideality factor of the base leakage current is close to 2. These data are consistent with the results reported in [22].

Figures 8 and 9 present the specific J_E and V_{CB} dependencies of the damage process, respectively. To reduce the error, three new devices are used for each stress conditions. The averaged base current damage ratios are compared at 0.5 V V_{BE}. In Figure 8 the base current damage ratio increases as J_E rises under fixed high V_{CB}. Based on the impact ionization mechanism, more injected carriers generate more "hot" electron-hole pairs if the impact ionization rate is fixed (i.e., fix V_{CB}), creating more traps at the surface of both oxides. Figure 8 also reveals a damage threshold that is found to be J_E = 20-30 mA/μm^2 at V_{CB} = 3.0 V.

Similarly, when V_{CB} rises, the electric field at the CB junction also rises, increasing the impact ionization rate and generating more hot carriers. As expected, Figure 9 shows such a trend with fixed J_E = 35 mA/μm^2 (fixed the injected carriers); as V_{CB} rises, the base current damage ratio increases. There is also a definable damage threshold: in this case V_{CB} = 0-1 V at 35 mA/μm^2.

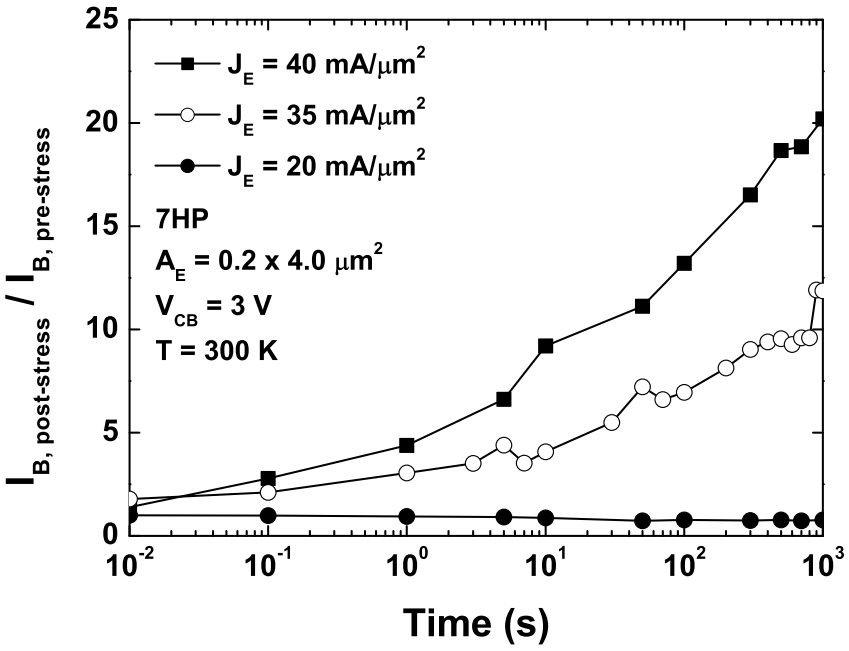

Figure 8: Base current damage ratio under forward-mode vs. stress time for different emitter current densities.

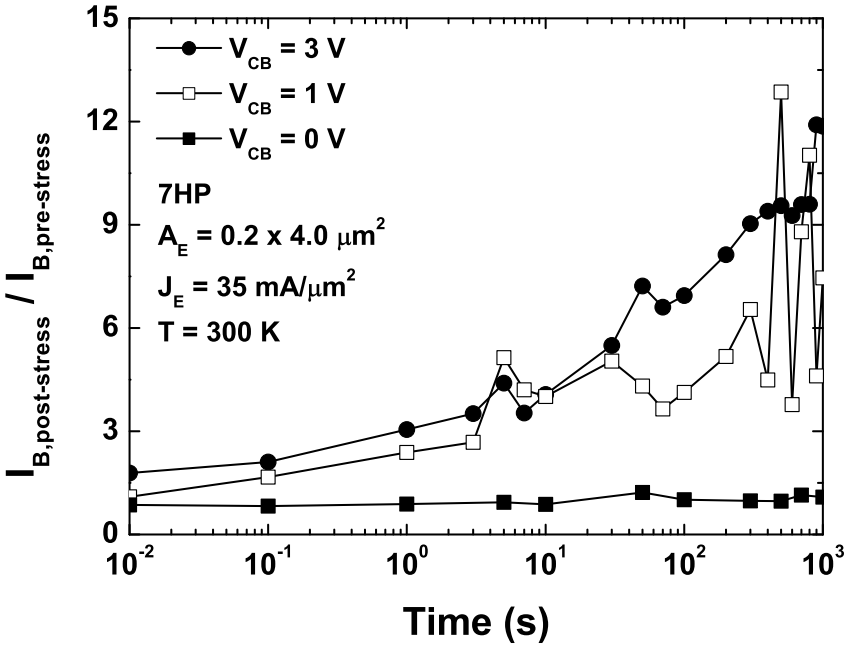

Figure 9: Base current damage ratio under forward-mode vs. stress time for different collector-base voltages.

Random fluctuations of the base current are consistently observed both within a single device and device-to-device at 1 V when J_E = 35 mA/μm^2 (see Figure 10). These fluctuations are likely

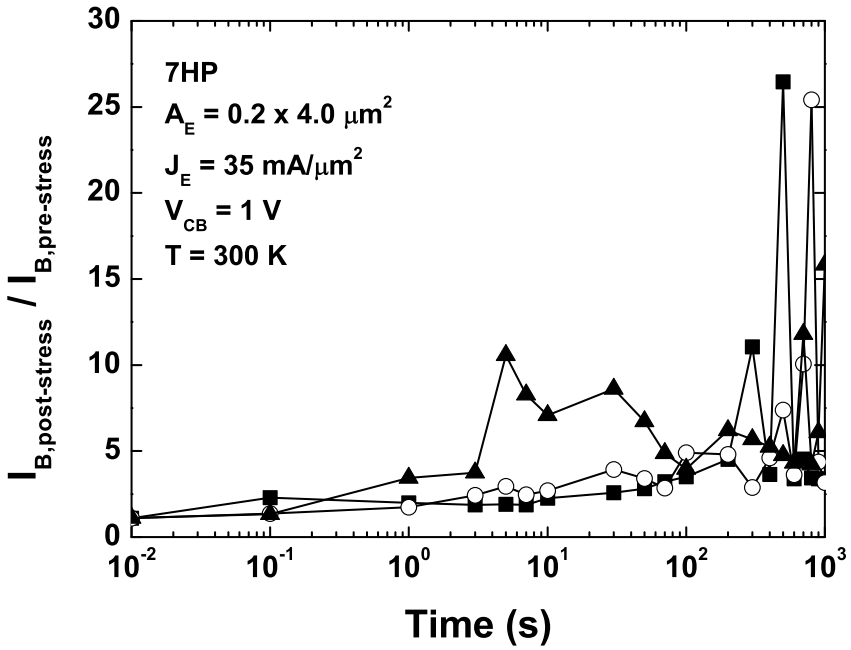

Figure 10: The bumpy base current damage ratio under forward-mode vs. stress time for J_E = 35 mA/μm^2 and V_{CB} = 1 V.

due to the simultaneous creation and annealing of stress-induced interface traps. In the next section (self-heating effect), this phenomenon will be explained with the damage threshold concept that found in terms of the current sweep stress.

Post-stress annealing studies were also performed for this study. As illustrated in Figure 11, the non-ideal component of the base current can be almost totally removed with a 400 °C anneal for 30 minutes in the forming gas. Again, this is consistent with the known behavior of interface traps. This result was repeated recently by another group [27], which performed a post-reverse-EB stress (open collector) anneal in addition to the post-MMS anneal. They demonstrated that the degradation resulting from reverse-EB stress could be annealed by a 250 °C forming gas, while MMS-induced degradation could not be annealed. These results suggest that MMS has a very different damage mechanism from reverse-EB stress, although hot carriers are involved in both.

To further understand the impact ionization process in MMS, special transistor test structures are designed with a variable shallow-trench (ST) to emitter (EM) spacing. All other device dimensions

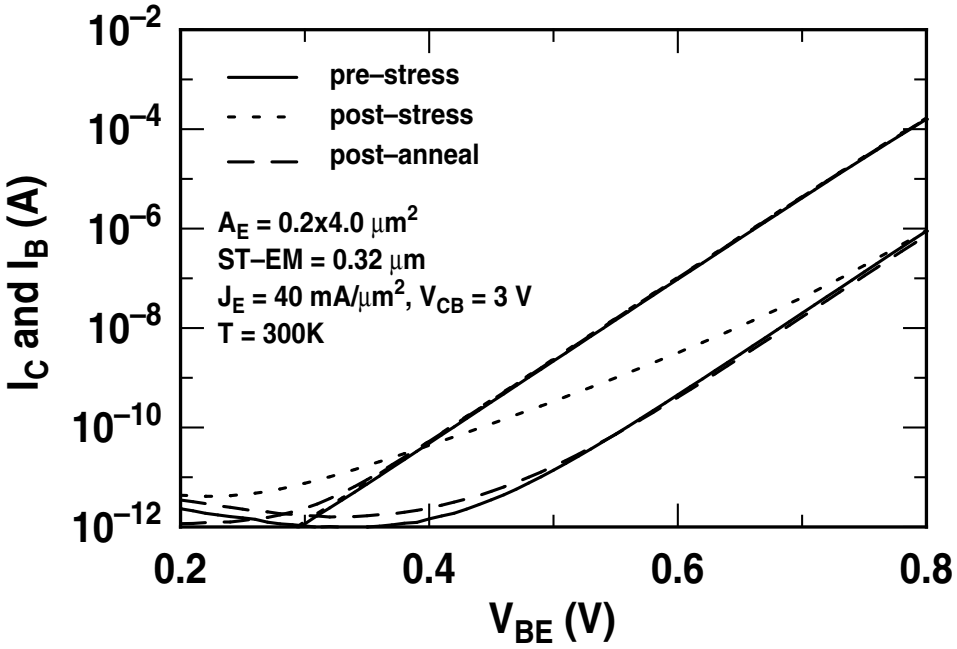

Figure 11: Forward-mode Gummel characteristics for pre-, post-stress, and post-annealing.

were fixed. The purpose of these structures was to shift the effective peak of the impact ionization in the CB junction laterally away from the emitter-base spacer (see the inset box in Figure 7). As shown in Figure 12, increasing the ST-EM distance strongly decreases the stress damage under fixed stress conditions. Figure 13 presents the normalized I_B degradation versus ST-EM distance under both forward-mode and inverse-mode operation after 1,000 seconds of cumulative stress. The I_B damage ratios decreased significantly under both modes with increasing ST-EM distance. These results demonstrate that the physical proximity of the location of the impact ionization with respect to the emitter-base spacer and shallow-trench edge is strongly correlated with the resultant mixed-mode degradation.

2.2.2 Low-Frequency Noise Degradation

Low-frequency noise is highly sensitive to the presence and position of G/R traps, and can thus provide additional insight into the damage mechanisms created by hot carriers [28].

Figure 14 provides a block diagram of the noise measurement setup used in this work. The system is composed of biasing circuits, two pre-amplifiers (model 5113), and one dynamic signal analyzer (Agilent 35670A) [29]. Devices are tested in the common-emitter mode. The biasing

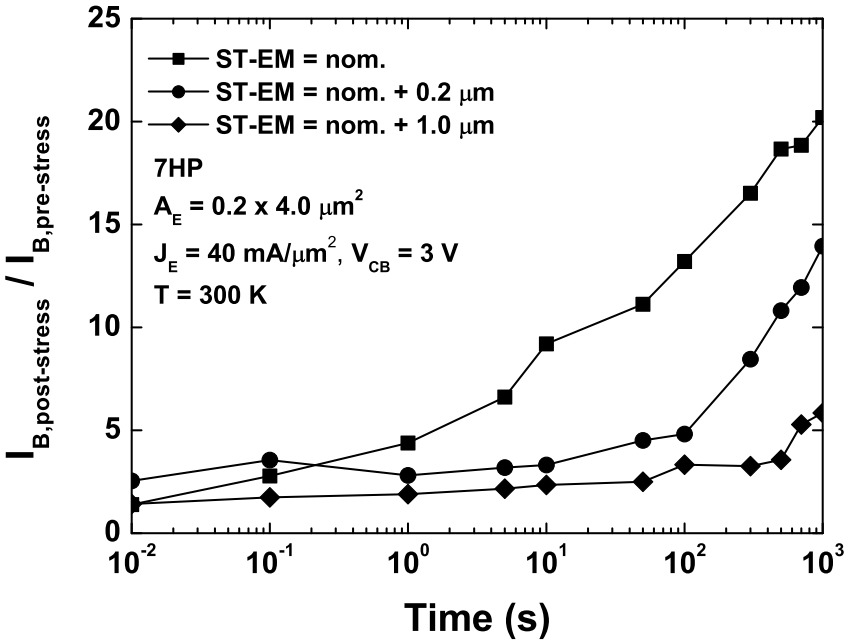

Figure 12: Base current damage ratio under forward-mode vs. stress time for different shallow trench (ST) to emitter (EM) spacing.

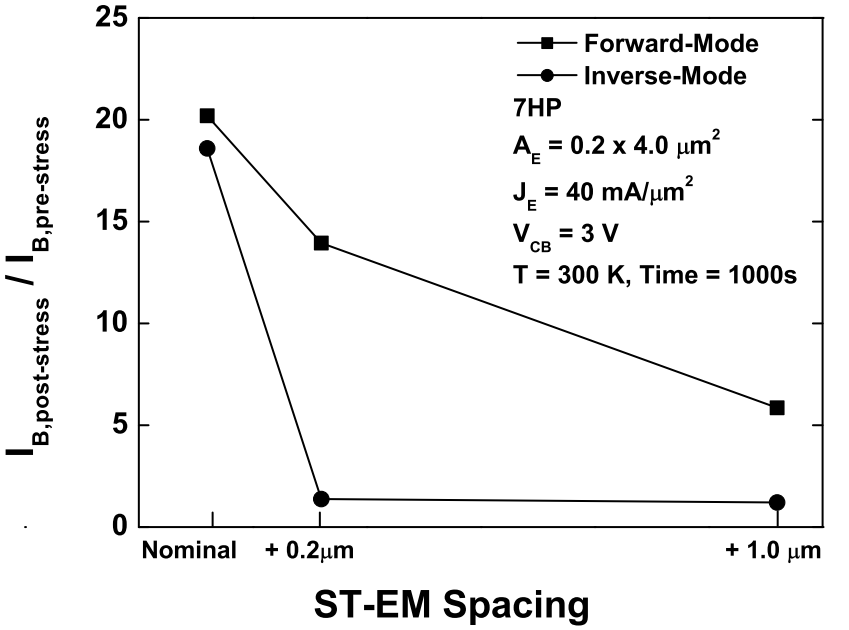

Figure 13: Base current damage ratio vs. ST-EM spacing under both forward-mode and inverse-mode.

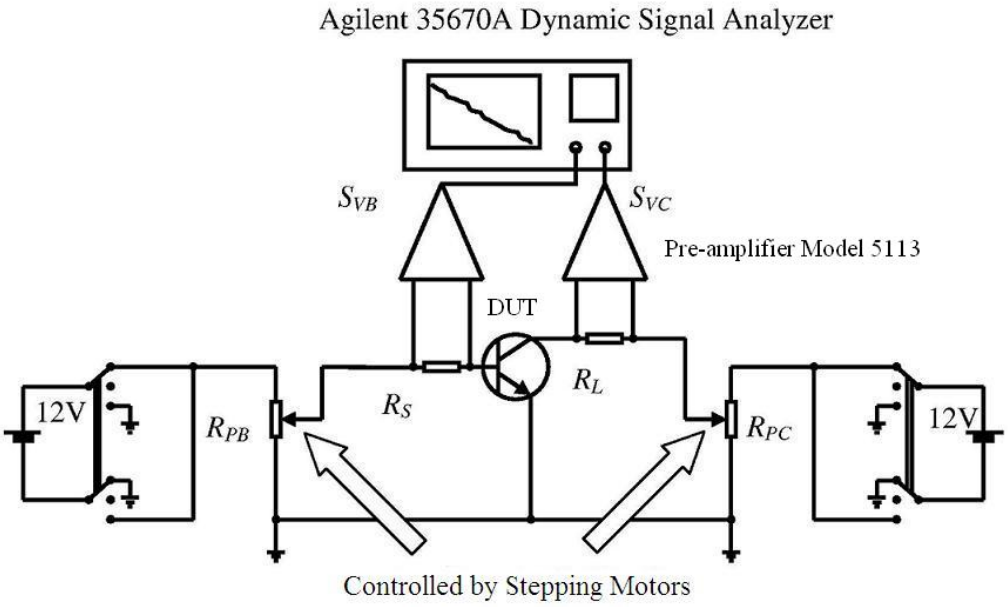

Figure 14: Noise measurement setup.

circuits use two 12 V lead acid batteries (Panasonic Model NO. LC-RD 1217P) to supply the biasing currents. The pre-amplifiers operate in the differential mode, with a gain of 500 and frequency roll-off to 6 dB between 0.03 Hz and 300 KHz. The dynamic signal analyzer records and analyzes the amplified noise signals within the frequency range from 1 Hz to 52 KHz. The base current noise power spectral densities were measured across two resistors series-connected with the base and the collector in the unit of V^2/Hz. The coherence between the two power spectral densities is normally close to unity for various reliability stresses, indicating that only one of the noise sources is dominant in the transistor. The noise generator S_{I_B} associated with the base is used to present the low-frequency noise data.

Figure 15 shows the input-referred noise spectra S_{I_B} at a bias current of 1 μA of SiGe HBTs with nominal ST-EM spacing before stress and after reverse-EB stress, as well as MMS. The measurements were taken from two to three sites from the same wafer for each type of stresses. The pre-stress noise spectra overlay very well for all devices. Hence, only one pre-stress curve is plotted in the figure for both stress methods. The results are quite interesting. The pre-stress low-frequency noise shows an ideal $1/f$ frequency dependence, while after reverse EB stress this changes to $1/f^{\alpha}$ noise with α close to, but slightly larger, than unity. This deviation from ideal frequency dependence

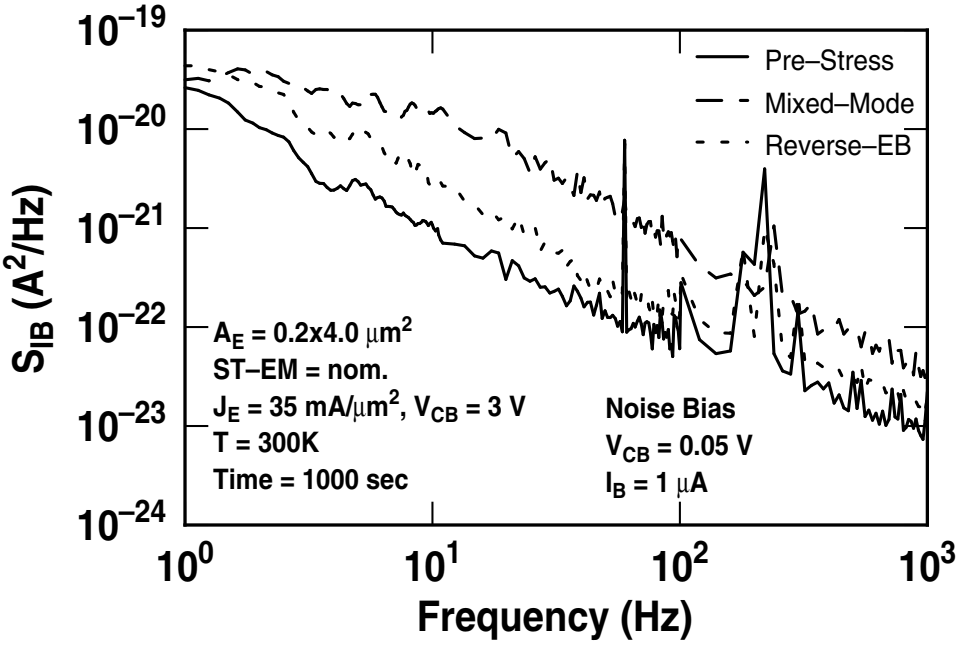

Figure 15: $1/f$ noise comparison among three different status: pre-stress, post reverse-EB stress, and post mixed-mode stress.

could be the result of thermally activated processes, as suggested by the Dutta-Horn model [30]. The noise spectra of some devices after MMS deviate from ideal behavior and exhibit a Lorentzian-shaped "hump," indicating the presence of significant G/R noise [31], and are different from those observed in reverse EB stress. Hence, reverse EB stress and MMS do not degrade the device identically, which implies fundamentally different damage mechanisms for the two different stress methods.

Noise measurements on transistors with different ST-EM spacing were performed in order to investigate the impact of ST-EM spacing on $1/f$ noise before and after stress. Figure 16 shows the normalized noise magnitude at 10 Hz as a function of ST-EM spacing. The normalized power spectrum decreases as the ST-EM distance increases. This is consistent with the *dc* data shown in Figure 12, indicating that larger ST-EM spacing produces less interface damage for the same stress conditions, and thus providing a potential mitigation path for mixed-mode damage effects.

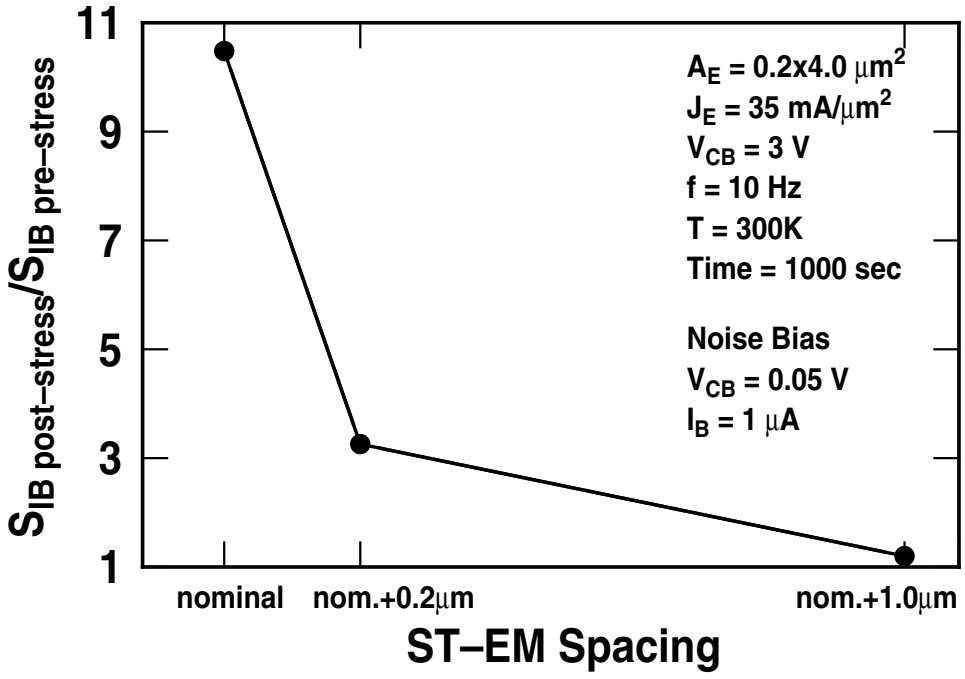

Figure 16: Noise spectrum ratio vs. ST-EM spacing.

2.3 Self-Heating Effect

As devices continue to scale down, the self-heating effect becomes more and more of a concern. The self-heating effect is the term used to describe the phenomenon of the junction temperature T_j rising as a result of scattering events, for example, impact ionization. In the impact ionization process, the carriers give up the energy they retain, generate phonons, and increase the magnitude of the lattice vibration, thus generating heat in the devices so that T_j rises. This self-heating effect can influence the device performance significantly since the device's characteristics are a function of the temperature. Device reliability can also be adversely affected by the elevated temperature, which promotes many damage mechanisms [32].

This section focuses on the self-heating issue for ultra-high power input during MMS. To calculate T_j, the thermal impedance is widely used. The thermal impedance is composed of thermal resistance (*dc* response) and thermal capacitance (*ac* response). In this study, only the *dc* response is a concern. Hence, the thermal resistance extraction method will be introduced before the discussion of the comprehensive experimental results.

2.3.1 Thermal Resistance Measurement

To characterize the self-heating effect, the junction temperature T_j is utilized since the principal heat source in Si BJT/SiGe HBT is the base-collector space charge region, or base-collector junction. The following formula is well accepted:

$$T_j = T_{amb} + R_{th} \times P_{diss} \tag{4}$$

where R_{th} is the thermal resistance, P_{diss} is the dissipated power, and T_{amb} is the ambient temperature. Since T_j is proportional to R_{th} for a given power consumption, it is very important to estimate the precise R_{th} of the device.

The R_{th} extraction method used in this study was developed by Rieh *et al.* [8]. The R_{th} is expressed from (4).

$$R_{th} = \frac{(T_j - T_{amb})}{P_{diss}} \tag{5}$$

A temperature-sensitive electrical parameter (TSEP) can be measured for various power dissipation levels to link the P_{diss} variation and temperature variation by a careful calibration. The most widely used TSEPs are the base-emitter voltage V_{BE} [33][34] and current gain β [35][36]. This study utilizes V_{BE} as TSEP. First, the device is biased with a fixed emitter current I_E and collector-base voltage V_{CB}, after which V_{BE} is measured for the substrate temperature T_S swept over the range of interest to produce the calibration curve (V_{BE} versus T_S). Second, the device is biased with the same I_E at fixed ambient temperature, and V_{BE} is recorded for different dissipated power with V_{CB} swept from -0.2 V to 1.0 V. The dissipated power can be calculated by

$$P_{diss} = I_C \times V_{CE} + I_B \times V_{BE} \tag{6}$$

For convenience, J_E is applied instead of I_E to facilitate the R_{th} extractions of devices with different sizes. J_E is set to be approximately half J_C at peak cutoff frequency. The criterion is that J_E should be not only high enough to show the self-heating effect, but also low enough to avoid device degradation, especially at high temperature. The V_{CB} range is moderate in order to avoid the avalanche effect. A setting of 0 V was chosen for this study.

By substituting (6) for (4) and eliminating V_{BE} from above two measurements, the obtained relationship between T_j and P_{diss} is very linear for constant R_{th} within the temperature range of

interest. The final step compensates for the self-heating effect in the first step. The first measurement links V_{BE} with the substrate temperature rather than T_j. Therefore, it is necessary to determine the y-axis intercept point (T_0) shown in Figure 17 and shift the entire line upward by an amount T_{amb}-T_0 [35] to obtain the final curve. R_{th} is the slope of this curve.

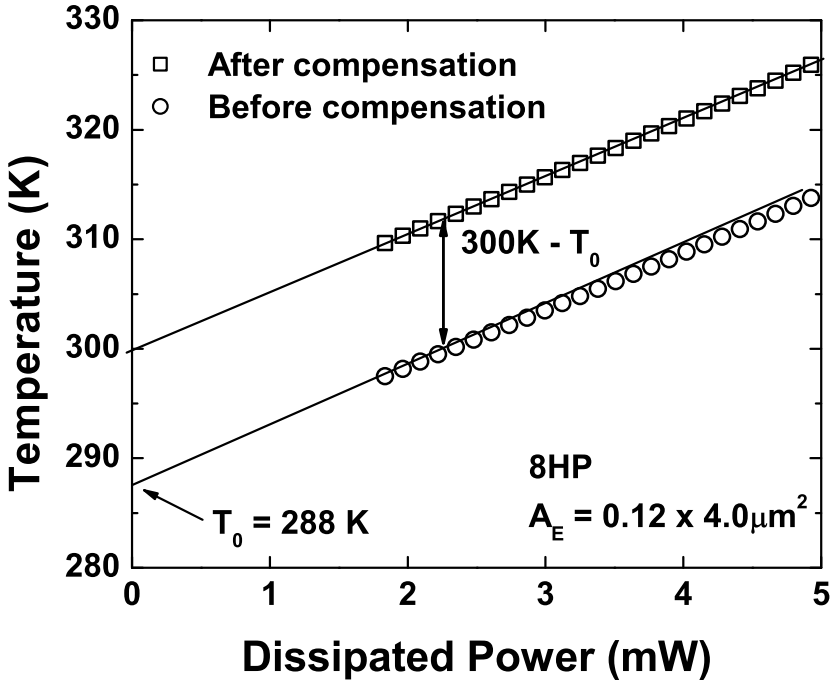

Figure 17: Junction temperature versus dissipated power before and after compensation.

2.3.2 Results and Discussion

The results presented in this section were collected by stressing the IBM's third-generation high-performance SiGe HBTs (8HP) with the current sweep stress (CSS) technique. Figure 18 shows the cross-section of the device [6]. Compared with the two older generations, the most significant structural improvement is that the 8HP SiGe HBT incorporates a raised extrinsic base patent. More details about this technology can be found in [6], and Section 2.1 provides a detailed description of the CSS technique.

Figure 19 illustrates the base current density from the forward-mode Gummels of the device under test (DUT) stressed with 3 V V_{CB}, a ten-second stress time interval, and an emitter current density J_E increasing from 0.142 mA/μm^2 to 98.40 mA/μm^2. The base current leakage can be

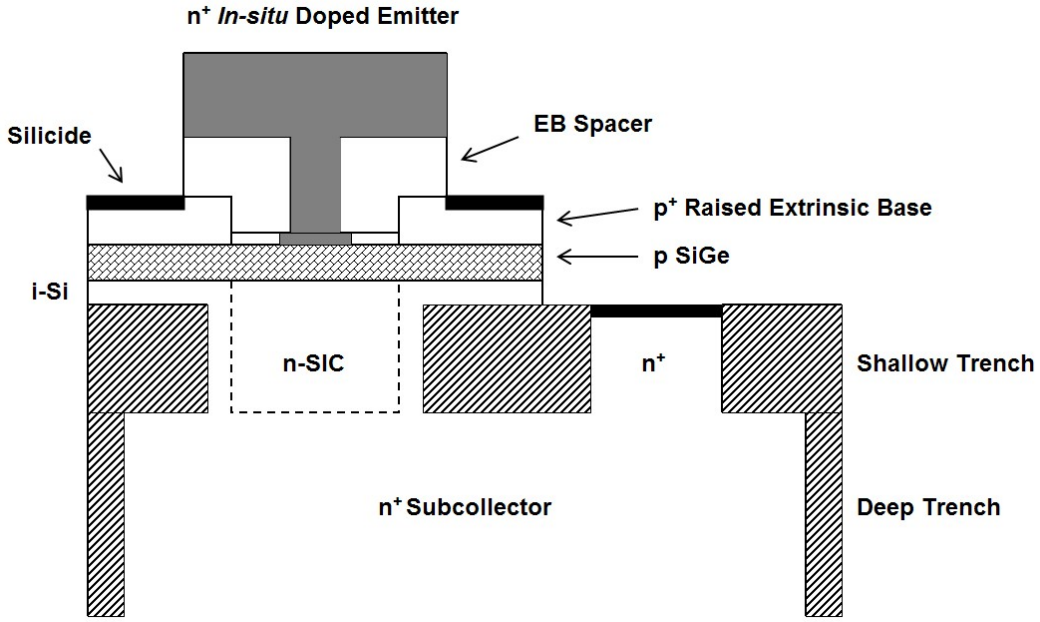

Figure 18: The cross-section of the IBM's third generation SiGe HBT.

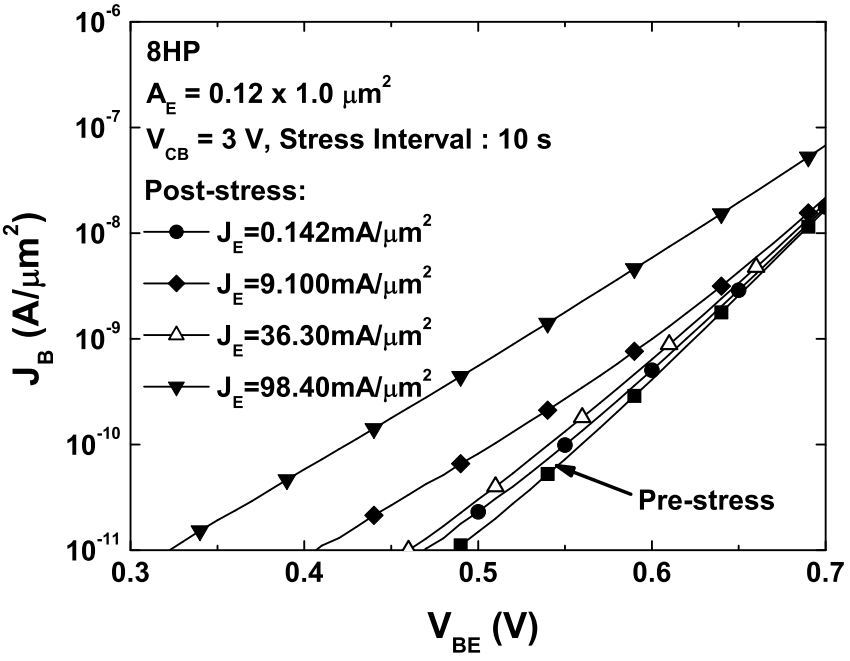

Figure 19: The base current density of the forward-mode Gummels during current sweep stress with $V_{CB} = 3$ V and $Time_{stress} = 10$ s.

observed even under conditions of very low current density stress (0.142 mA/μm^2). The leakage current increases with increasing stress current (9.10 mA/μm^2), followed by a decrease as J_E continues to increase (36.30 mA/μm^2). Finally, the leakage current increases rapidly at a stress current of 98.40 mA/μm^2.

Figure 20 clearly demonstrates this trend in the relation between base current damage ratio (V_{BE} = 0.5 V unless specified otherwise) and the stress current density J_E. This relationship is termed the

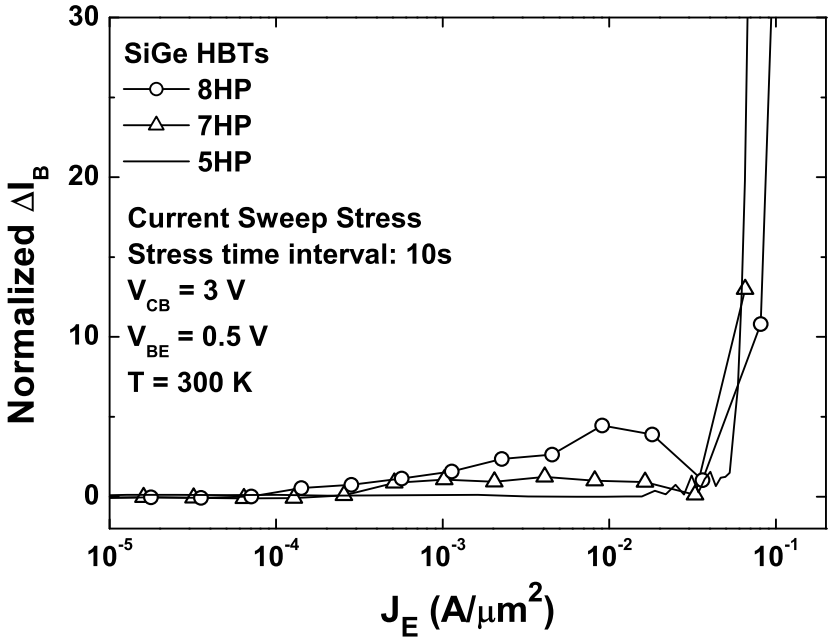

Figure 20: Base current damage ratios at $V_{BE} = 0.5$ V versus stress current J_E, or damage spectrum, across IBM's SiGe HBT generations

forward mode damage spectrum since it is extracted at fixed V_{BE} from the forward-mode Gummels recorded after each stress point. Another damage spectrum can be plotted from the inverse-mode Gummels, which is termed *inverse mode damage spectrum*. In the following discussion, the damage spectrum indicates the forward mode unless otherwise stated. The shape of the damage spectrum includes three main parts: a "hump" region, a "rapid increase" region, and a threshold between these two regions [25].

The hump region can be divided into two parts: low-current damage (rising side) and mixed-mode anneal (falling side). The hump peak for the 8HP DUT is around 10 mA/μm^2, as illustrated in Figure 20. The hump is repeatable across both 7HP and 8HP SiGe HBTs, although there is no

significant hump for 5HP devices. Based on the stress current level, the rising part of the hump occurs as a result of the impact ionization-induced hot carriers that generate the G/R traps at the EB spacer [37][38]. Hence, as expected, the hump peak magnitude follows the sequence: 8HP > 7HP > 5HP, which is also the sequence of the impact ionization level across the device generations. The mixed-mode anneal is a self-heating induced thermal anneal [25]. The higher the stress current applied, the higher the T_j produced and the more traps annealed, and the lower the base current degradation ratio observed. The details about the hump region study can be found in [25].

Rapid increase regions are common for all three generations of devices, and this is referred to as high current damage. The I_B degradation ratio exhibits a linear-like dependence with J_E on a logarithm scale. The MMS conditions discussed in Section 2.2 belong in this region, indicating a different degradation mechanism from that at low current damage.

The threshold is the transition point from the mixed-mode anneal region to the high current damage region. The current density at the threshold can be obtained by plotting the damage spectra in a log-log scale. In Figure 20, the threshold point is around 30 mA/μm^2 for 7HP. This result is consistent with the damage threshold discussed in Section 2.2.1. When DUTs are stressed around this threshold by the time cumulative method, due to the strong trap generation (high current damage) and anneal (mixed-mode anneal), a bumpy spectrum (see Section 2.2.1) is expected. Later discussions point out that the self-heating effect also plays a very important role in the determination of the threshold point.

To study the self-heating impact on MMS, I designed a series of experiments by current sweep stress technique to stress a family of 8HP SiGe HBTs with the same emitter width, but different emitter lengths. As noted in Section 2.3.1, shorter devices are known to exhibit larger thermal resistance. The self-heating effect thus can be distinguished easily from the impact ionization effect since they have the same $M - 1$ curves. Figure 21 clearly shows this trend in thermal resistance for various emitter lengths and Figure 22 compares the damage spectra for these DUTs. The high current damage regions shift almost in parallel for these DUTs. The longest device (0.12 × 8.0 μm^2) has the smallest J_E at the threshold and the shortest (0.12 × 1.0 μm^2) has the highest threshold. However, considering I_E values at the threshold the situation is reversed, as shown in Figure 23. The junction temperatures were calculated for all DUTs at their thresholds by $T_{junction}$

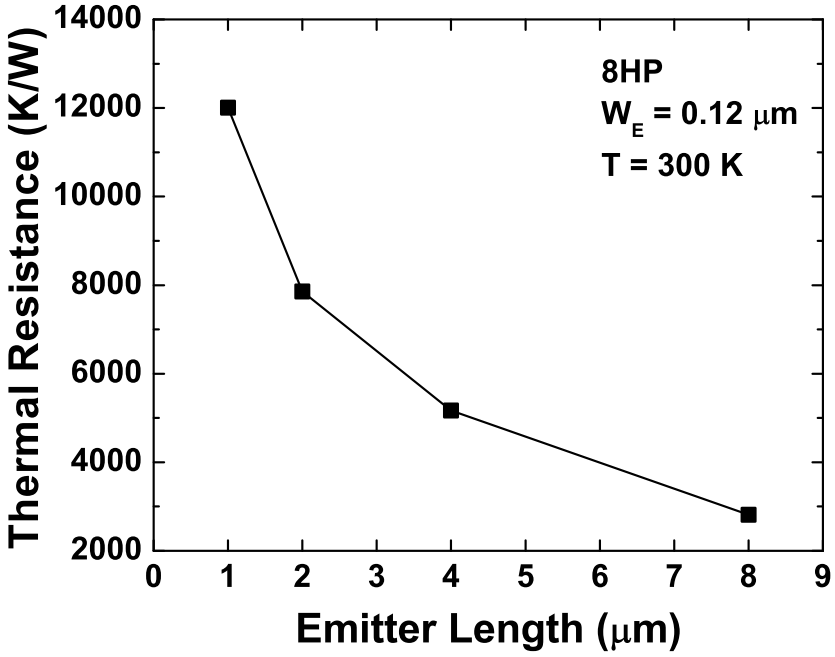

Figure 21: Thermal resistances of 8HP SiGe HBTs for various emitter lengths.

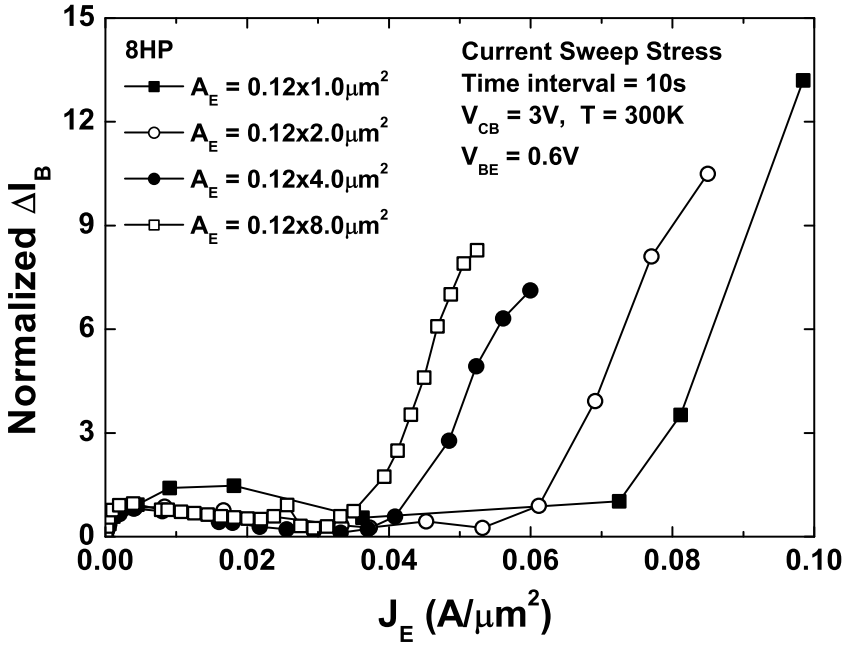

Figure 22: Damage spectra of 8HP SiGe HBTs for various emitter lengths.

$\approx T_{ambient} + R_{th} \times I_E V_{CE}$. The calculations show the junction temperatures are very close to each other, at around 720 K - 730 K, suggesting thermal dependence.

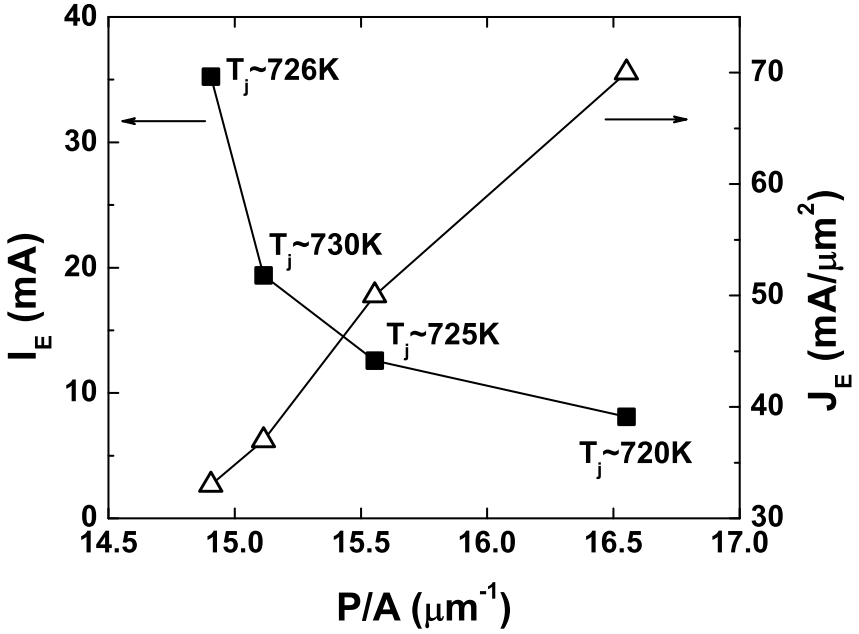

Figure 23: The I_E and J_E at the threshold versus DUTs' perimeter-to-area ratios.

To verify the threshold, the 0.12 μm× 8HP SiGe HBT family was stressed by the time cumulative stress technique. The current density was carefully chosen to be in the high current damage region for the 0.12 μm×4.0 μm DUTs, but below the threshold for both the ×1.0 μm and ×2.0 μm DUTs. As expected, the first DUTs suffered more degradation than the other two DUTs, as shown in Figure 24.

The threshold shift provides a good explanation of the perimeter-to-area ratio (P/A) issue reported in [22]. As is well known, the base current can be separated into a function of the peripheral component I_p and the internal base current component I_i as follows under normal bias conditions:

$$I_B = I_i + I_p \approx A_E C_i e^{\frac{qV_{BE}}{kT}} + P_E C_p e^{\frac{qV_{BE}}{kT}} \tag{7}$$

where A_E is the emitter area, P_E is the perimeter of the emitter area, and C_i and C_p are two constants for the internal component and the peripheral component, respectively. Dividing both sides of the equation by A_E for a fixed V_{BE} and T, then

$$J_B = C_1 + C_2 \frac{P_E}{A_E} \tag{8}$$

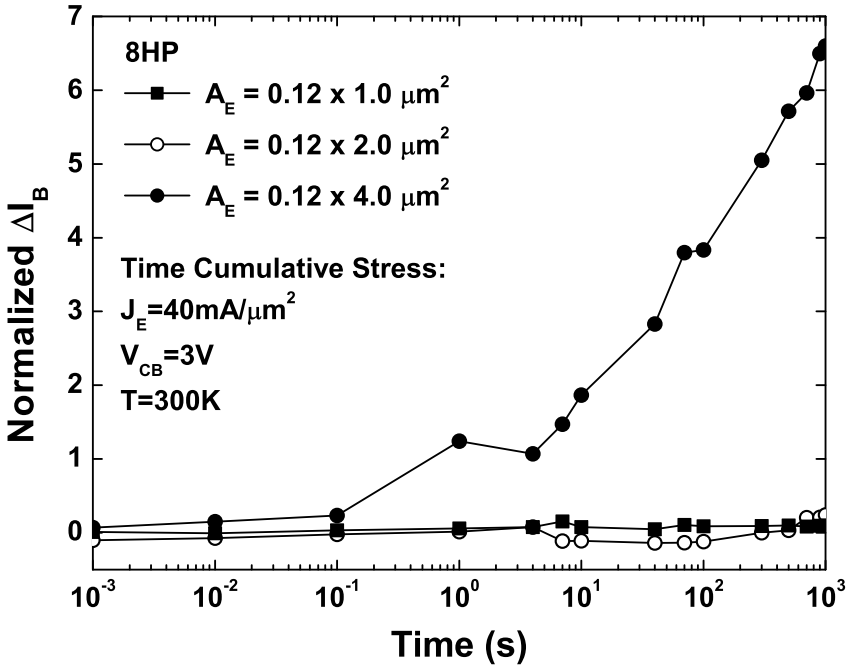

Figure 24: The base current damage ratio versus time for various emitter sizes.

Theoretically, J_B is proportional to P/A if the peripheral component is dominant, while J_B is independent of P/A if the internal component is dominant. Figure 25 compared the base current leakage versus the perimeter-to-area ratio before and after reverse-EB stress and MMS [22]. The stress conditions are: mixed-mode stress, J_C = 10 mA/μm^2 and V_{CB} = 4 V; reverse-EB stress, collector open, V_{EB} = 3 V, and t = 100 second. Stress-induced traps are known to be located at the EB spacer for both reverse-EB stress and MMS, and the leakage current resulting from these traps, which is the peripheral component, is dominant in low V_{BE} range. Therefore, the J_B is almost a constant before the stress is applied in both cases, and increases as P/A increases after reverse-EB stress. However, MMS showed a different trend with J_B inversely proportional to P/A. The reason for this is clear by an examination of the data in Figure 23 where if the stress current density is fixed, a longer DUT will have a higher damage ratio than a shorter DUT, and thus a higher J_B with a smaller P/A.

Additional measurements compared the damage spectra of the DUTs with the same size and generation at 200 K and 300 K. Figure 26 shows that the threshold for damage spectra shifted toward a higher number as temperature decreased, suggesting that the threshold is a function of

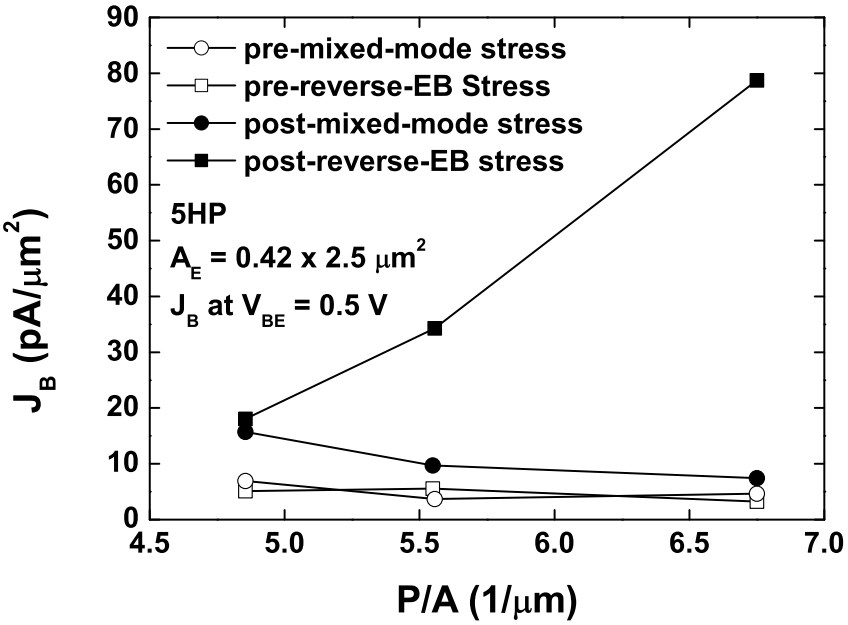

Figure 25: Base current density versus perimeter-to-emitter ratio for pre- and post- reverse-EB stress and mixed-mode stress. Mixed-mode stress condition: $J_C = 10$ mA/μm^2, $V_{CB} = 4$ V. Reverse-EB stress condition: collector open, $V_{EB} = 3$ V, t = 100 sec. After [22]

temperature.

The threshold can explain a generation issue that has puzzled the researcher for some time [23]. The same J_E and V_{CB} were stressed: one of which was a 7HP device with $A_E = 0.2 \times 4.0$ μm^2 and the other an 8HP device with $A_E = 0.12 \times 4.0$ μm^2. The results showed that the base current damage ratio for the 7HP DUT was much higher than that of the 8HP DUT, as shown in Figure 27. The damage ratio of the 8HP DUT was surprisingly much lower than that of the 7HP DUT, which is contrary to what would be expected for the impact ionization behavior. However, by taking the threshold into account, the answer became clear. Although the same J_E was applied to both, for the 7HP DUT this J_E falls into the high current damage region, while for the 8HP DUT this J_E is in the mixed-mode anneal region. Figure 20 shows that 8HP devices can also have a comparable current leakage level to 7HP devices when the applied J_E is high enough. The results suggest that the trend of scaling becomes uncertain in MMS due to the threshold.

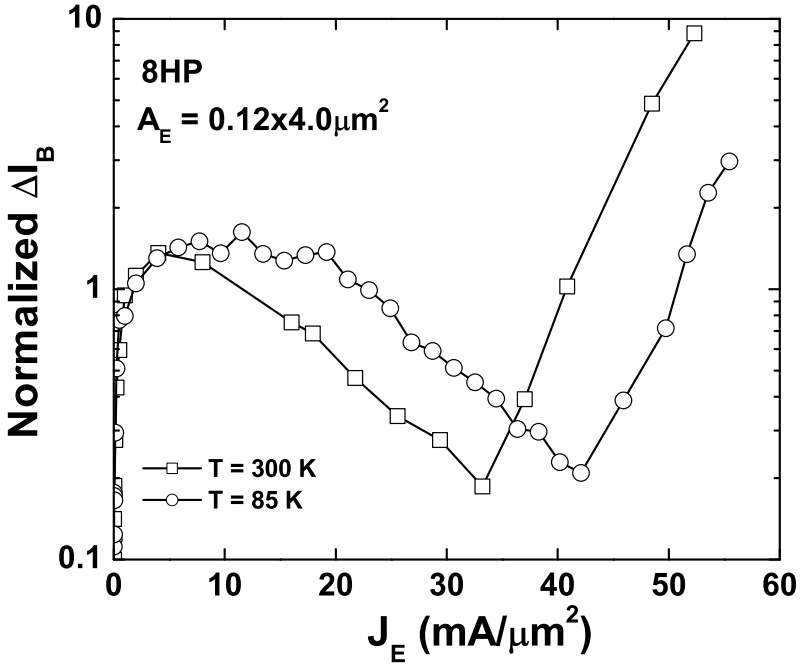

Figure 26: 8HP SiGe HBTs damage spectra plotted from forward-mode Gummels at 200 K and 300 K.

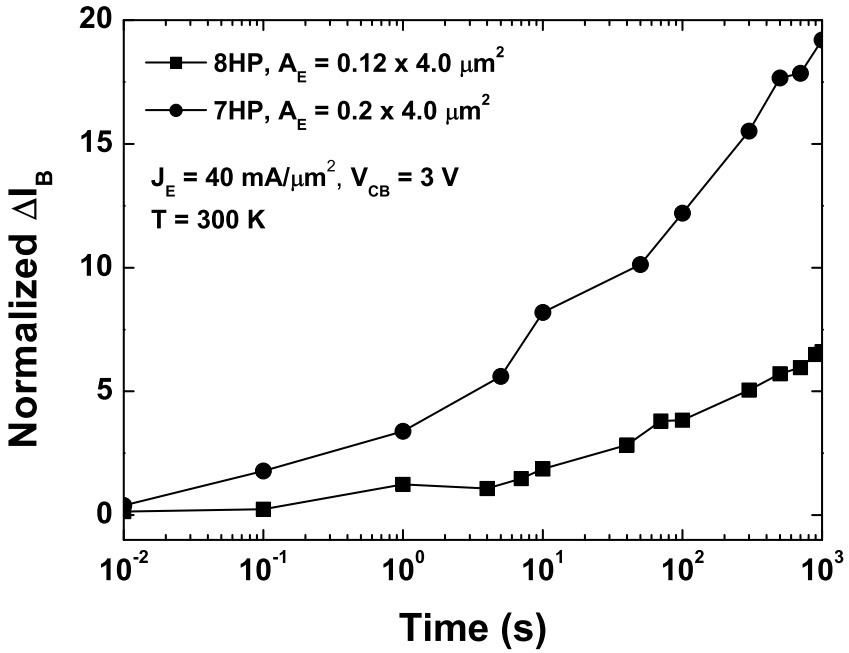

Figure 27: Excess base current for 7HP (120 GHz peak f_T) and 8HP (208 GHz peak f_T) SiGe HBTs stressed with the same J_E and same V_{CB}.

2.4 Summary

In this chapter, the damage mechanism of MMS was investigated using two stress techniques: time cumulative stress and current sweep stress. Both of these techniques applied current density J_E and voltage V_{CB} on the DUTs, forcing the DUTs to operate in forward mode. The study revealed that not only impact ionization, but also self-heating induces MMS degradation.

According to the time cumulative stress results, the damage is clearly located at both the EB spacer and STI edge. The J_E, V_{CB}, and emitter-to-shallow trench isolation spacing dependences all indicate that impact ionization and the proximity of the emitter-base spacer to the region of strongest impact ionization both play a strong role in the damage process. Noise and post-MMS anneal measurements demonstrate that reverse EB stress and MMS have fundamentally different damage mechanisms. The noise data confirm the importance of ST-EM spacing in MMS.

The recently developed current sweep stress technique was used to assess the role of the self-heating effect in MMS by conducting stress tests on the same generation DUTs but with different geometries, producing a series of damage spectra. The results showed that the damage threshold (in current density) increases for shorter devices because of the different R_{th}. These results explain both the P/A issue raised in [22] and the generation issue in [23]. The damage spectra at various temperatures further confirm the different degradation mechanisms between low current damage regions and high current damage regions.

CHAPTER III

DEVICE SIMULATIONS

3.1 Introduction

The growing need to understand basic device operation, to optimize device structures, and to consider novel device structures has led to a new emphasis on the importance of numerical device simulation. Numerical analysis based on the fundamental differential equations governing semiconductor is widely used, for example the powerful device simulator, MEDICI, which is utilized here. MEDICI is an industry-standard device simulation tool developed by Synopsys to predict the electrical, thermal, and optical characteristics of semiconductor devices using a range of advanced physical models, e.g. Shockley-Read-Hall and Auger recombination models, avalanche, bandgap narrowing, Fermi-Dirac and Boltzmann statistics, gate current, and various mobility models. A wide variety of devices can be modeled in one, two, and/or three dimensions, including MOSFETs, BJTs, HBTs, SOI, and power devices, etc. Figure 28 illustrates the MEDICI simulation procedure schematically.

In the first step, a model device is built in the simulator using designed and measured process data, such as the layout and SIMS profile. The measured SIMS profile for the first generation SiGe HBT is shown once again in Figure 29, while Figure 30 shows the net doping profile used for the device simulation. Comparing the two figures, the most obvious difference is the arsenic segregation peak at the polysilicon/silicon interface in the measured SIMS data. However, this is not a real feature due to the finite resolution limit of the SIMS measurement technique when the arsenic doping profile changes rapidly [1]. Had this peak been correct, there would be no p-type base in the SiGe HBTs.

After inputting the SIMS data, the second step is to construct and refine a grid structure on the device for numerical analysis. Figure 31 shows a cross-section of the SiGe HBT device used in the simulator. The structure is identical to the investigated SiGe HBT technology. Figure 32 illustrates the meshed structure. Note that a non-uniform gridding technique is implemented to

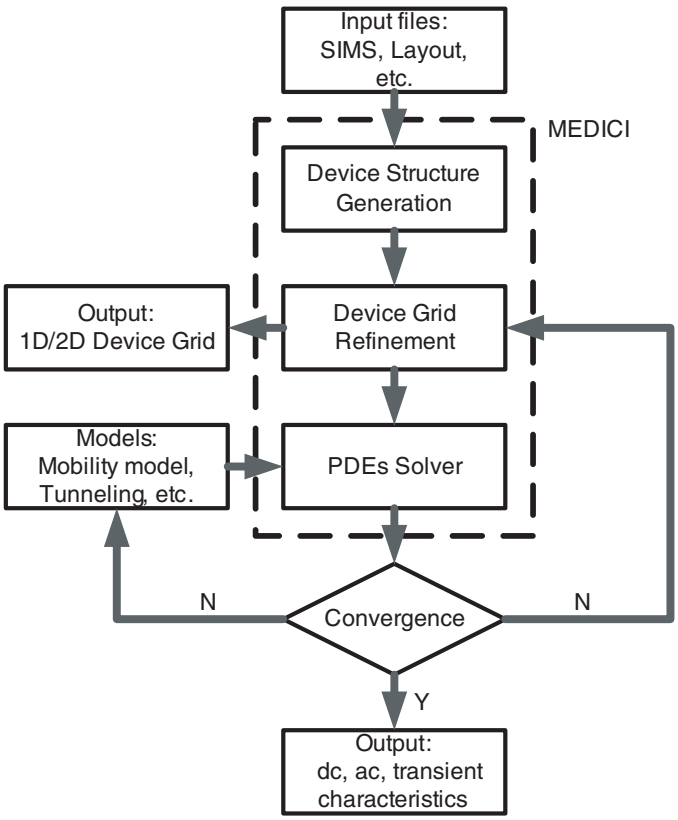

Figure 28: MEDICI simulation procedure.

reduce computation time and improve simulation accuracy; fine grids are used at junctions (EB and CB) and the regions near two oxides (EB spacer and STI), while far away from those regions, coarse girds are acceptable.

The third step is to specify and solve the partial differential equations (PDEs) using calibrated parameter models. The PDEs include six equations, listed below [39]:

$$\epsilon\nabla^2\psi = -q(p - n + N_D^+ - N_A^-) - \rho_S, \tag{9}$$

$$\frac{\partial n}{\partial t} = \frac{1}{q}\vec{\nabla}\cdot\vec{J_n} - U_n = F_n(\psi, n, p), \tag{10}$$

$$\frac{\partial p}{\partial t} = \frac{1}{q}\vec{\nabla}\cdot\vec{J_p} - U_p = F_p(\psi, n, p), \tag{11}$$

$$\rho c\frac{\partial T}{\partial t} = H + \vec{\nabla}\cdot(\lambda(T)\vec{\nabla}T), \tag{12}$$

$$\vec{\nabla}\cdot\vec{S_n} = \frac{1}{q}\vec{J_n}\cdot\vec{E} - \frac{3}{2}[n\frac{u_n - u_0}{\tau_{wn}} + \frac{\partial(nu_n)}{\partial t}] - \frac{1}{q}E_g G_n^{II} + H_n^R, \tag{13}$$

$$\vec{\nabla}\cdot\vec{S_p} = \frac{1}{q}\vec{J_p}\cdot\vec{E} - \frac{3}{2}[p\frac{u_p - u_0}{\tau_{wp}} + \frac{\partial(pu_p)}{\partial t}] - \frac{1}{q}E_g G_n^{II} + H_p^R \tag{14}$$

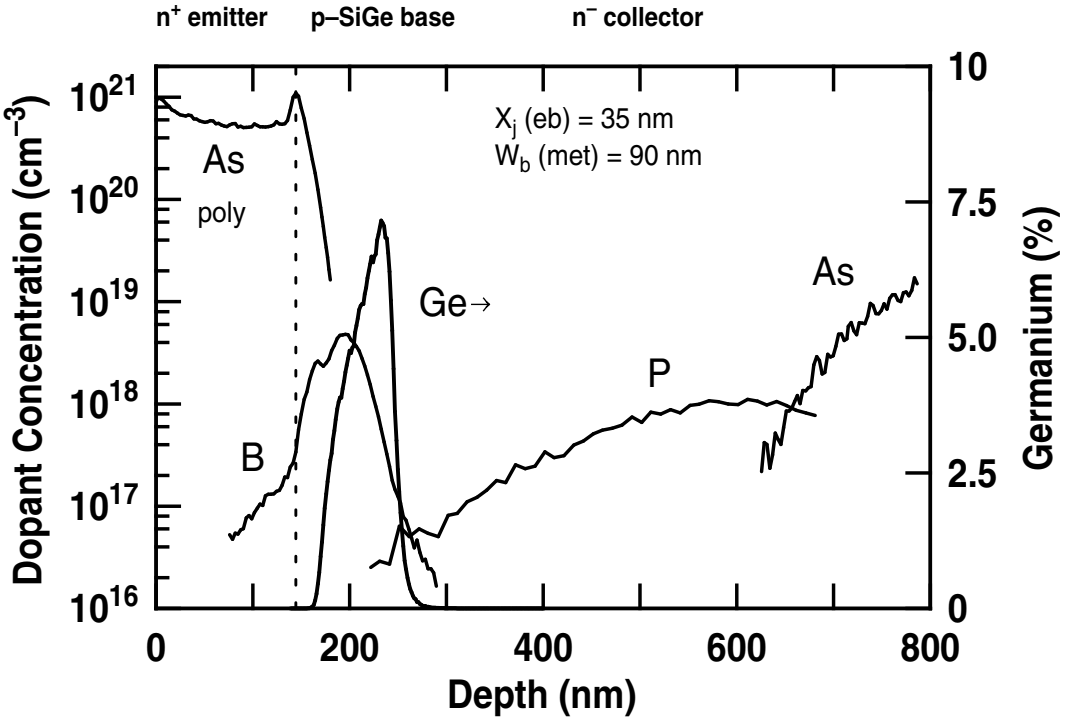

Figure 29: Typical doping profile measured by SIMS for a first-generation SiGe HBT.

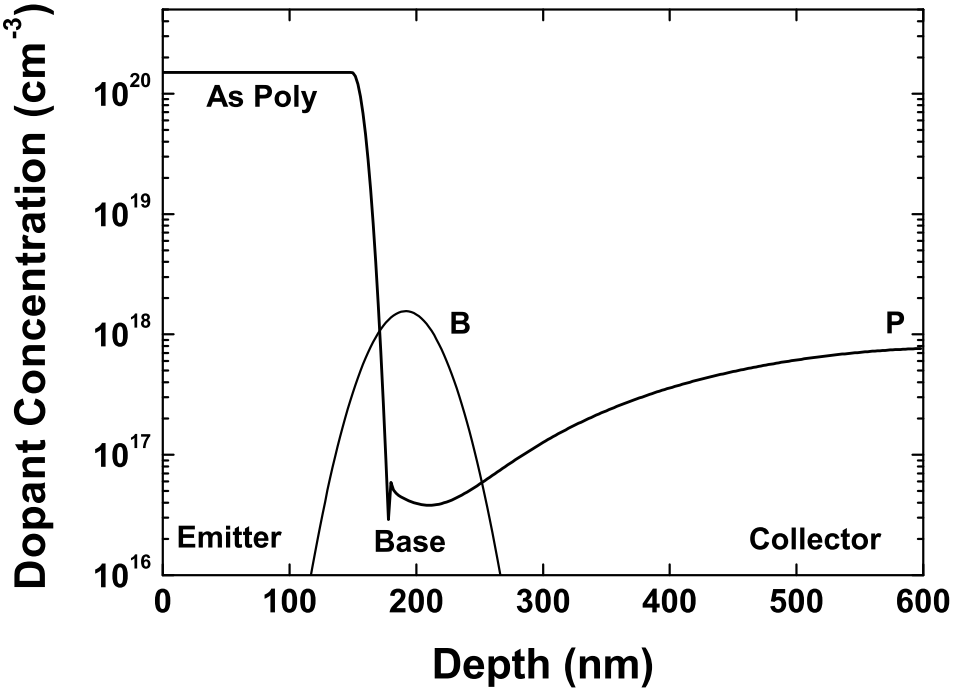

Figure 30: Typical doping profile of a first-generation SiGe HBT used for MEDICI simulations.

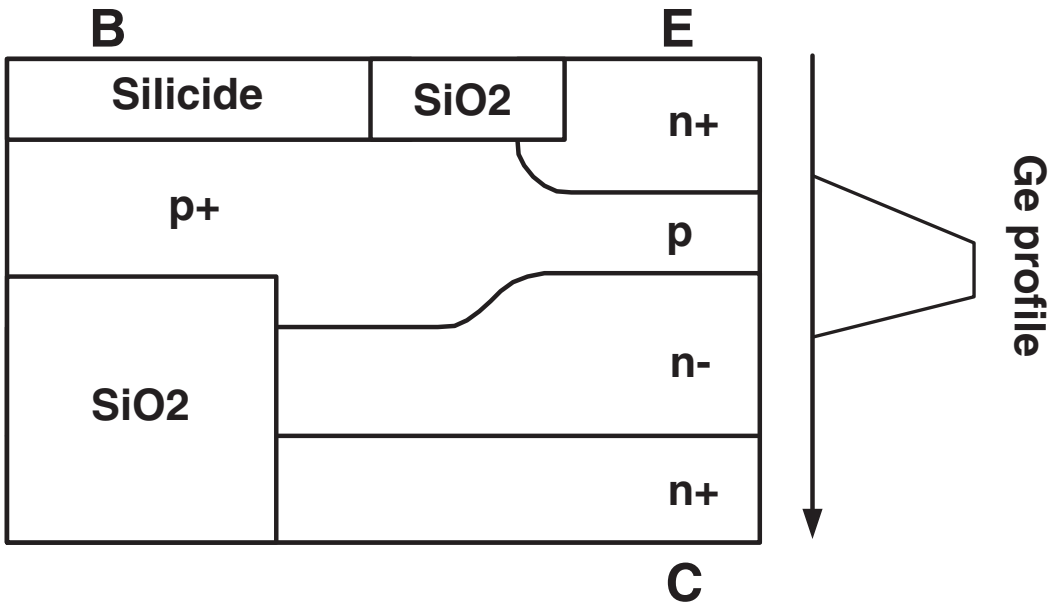

Figure 31: Schematic cross-section of the SiGe HBT in the MEDICI simulations.

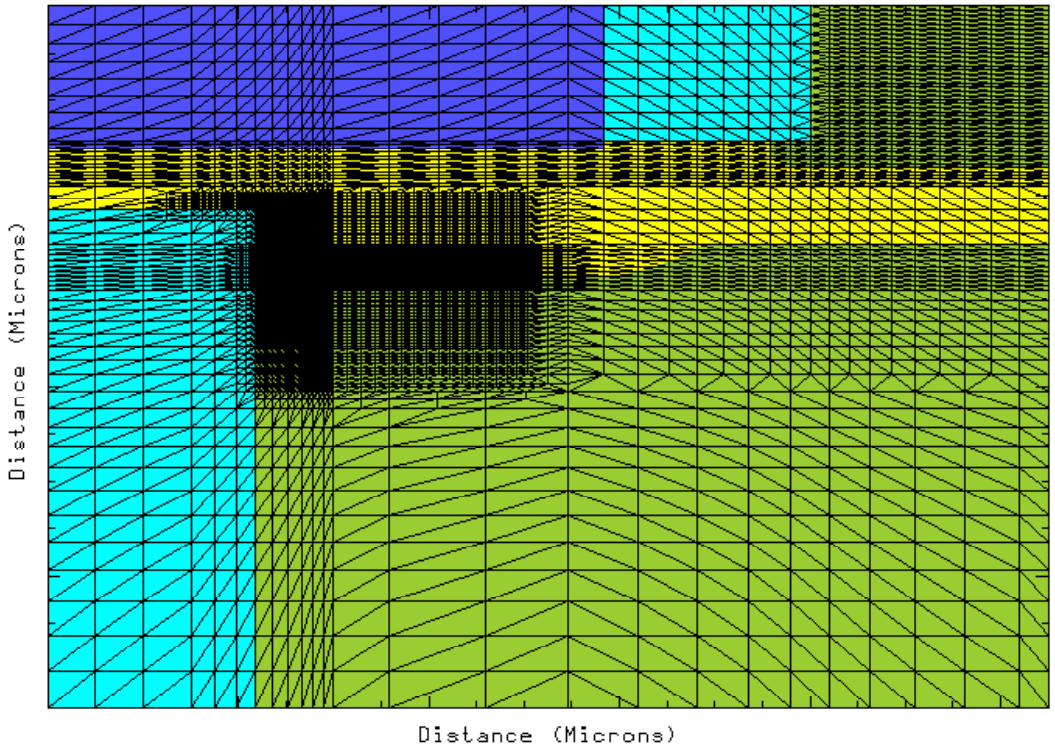

Figure 32: The 2D meshed SiGe HBT structure.

The first of these equations is Poisson's equation, while the next two are the electron/hole current continuity equations, respectively. The fourth equation describes the lattice heat continuity. The final two equations are electron/hole energy balance equations, respectively. In the above equation arrays, ψ, n, p, T, u_n and u_p represent the potential, electron/hole density, temperature, and electron/hole energy, respectively. They are six fundamental unknown distribution functions that can be used to link the other variables in the equations by applying appropriate physics models. To numerically solve these PDEs, the equations must be discretized with the meshes. Thus, if the total numbers of grid cells is N, MEDICI has to solve $6N$ real values. MEDICI can turn the models on/off and change model parameters if necessary for simulations. The consequent results can then be studied to determine the most effective way to decouple the device physics effects.

A frequent problem in device simulation is the convergency issue where the PDE solver is unable to obtain a convergent result for the equations. Typical methods to address this include: 1) mesh size adjustment, which involves going to a finer grid; 2) model modification, by turning on/off some models or changing model parameters. Once convergence has been achieved, MEDICI saves the solution, and outputs the *dc*, *ac*, and transient responses.

3.2 Carrier Transport Models

Since Gummel [40] first suggested a fully numerical model for a one-dimensional bipolar transistor based on the partial differential equations proposed by Van Roosbroeck [41] forty-two years ago, numerical solutions have been extensively investigated and continuously improved. Today, device simulations have covered a wide variety of devices and models. Of particular interest are the carrier transport models. Three carrier transport models are now generally used: the drift-diffusion (DD) model, the hydrodynamic (HD) model, and the Monte Carlo (MC) model. These will be briefly introduced here.

The standard DD model is derived from the Boltzmann transport equation (BTE), which introduces macroscopic parameters (e.g. mobility, diffusivity) assuming of a quasi-thermal equilibrium distribution [42]. The standard DD model is sufficient for low field transport with no rapidly varying spatial inhomogeneities. However, it alone is not well suited to analyze issues in modern semiconductor devices (e.g. high field transport, or "hot" carrier) because the carrier energy, which is the

most important factor, is not included in the DD approach. In spite of this disadvantage, the DD model is still used to provide an initial guess in many simulations.

The MC technique has now been used now for over 30 years, and many publications describing this approach can be found anywhere. The basic MC algorithm is based on the individual representation of a significant portion of the charge carrier population as computer particles [43]. Hence, one advantage of this technique is its ability to depict a complete picture of carrier dynamics based on their microscopic material parameters, such as effective masses and coupling constants. If this particle based simulation incorporates a numerical rather than an analytical representation, the band structure directly into the particle dynamics and scattering was then introduced. This method is commonly termed a full-band Monte Carlo simulation (FB-MC). FB-MC simulation is considered to be the most accurate approach within the framework of semi-classical device physics [44][45]. However, although the MC approach has enjoyed considerably success for device simulations, it is not widely used due to its unattractive computing time.

The HD model was developed by Rudan and Odeh in 1986 [46]. During the past twenty years, many researches have implemented this model since it is not only much faster than FB-MC but also accurate enough for device simulations. The HD model treats the propagation of carriers (electrons, holes) in a semiconductor device as the flow of a charged compressible fluid [47]. The model incorporates hot carrier effects that are missing in the standard DD model, such as velocity overshoot. In the HD model, the electron density, momentum and energy conservation equations for electron transport can be written in the following forms [48]:

$$\frac{\partial n}{\partial t} = \frac{1}{q}\nabla \cdot J_n - U \tag{15}$$

$$J_n = q\mu_n n\zeta + k_B\mu_n m_n \nabla(\frac{nT_n}{m_n}) + n\mu_n m_n \frac{dv_n}{dt} \tag{16}$$

$$\nabla \cdot S_n = \zeta \cdot J_n + w_n U - \frac{n(w_n - w_0)}{\tau_{w_n}} - \frac{\partial(nw_n)}{\partial t} \tag{17}$$

where n is the electron density, v_n is the mean velocity, T_n is the temperature, τ_{w_n} is the electron energy relaxation time, μ_n is the electron drift mobility, U = R - G is the net recombination-generation rate, k_B is the Boltzmann constant, J_n is the electron current density, ζ is the electric field and S_n is

the electron energy flow density:

$$S_n = H_n - \frac{J_n}{q}(w_n + k_B T_n) \tag{18}$$

where H_n is the electron heat flux. w_n is the electron energy which is given by

$$w_n = \frac{1}{2} m_n v_n^2 + \frac{3}{2} k_B T_n \tag{19}$$

These, along with Poisson's equation, form the HD model.

However, as the device feature size scales down, the validity of the DD model and HD model becomes questionable. For instance, in state-of-the-art SiGe HBTs, the base thickness can be 20nm or even thinner. When the length of the quasi-neutral base region shrinks to dimensions that are of the same order as the mean free path between collisions, macroscopic parameters (e.g. mobility) that involve numerous collisions within the quasi-neutral region become meaningless due to insufficient scattering of carriers, and nonequilibrium effects like velocity overshoot become very noticeable. Fortunately, many studies have demonstrated that the HD model is still reliable for advanced SiGe HBT simulations. Figures 33 and 34 show the vertical profiles of electron density and mean electron

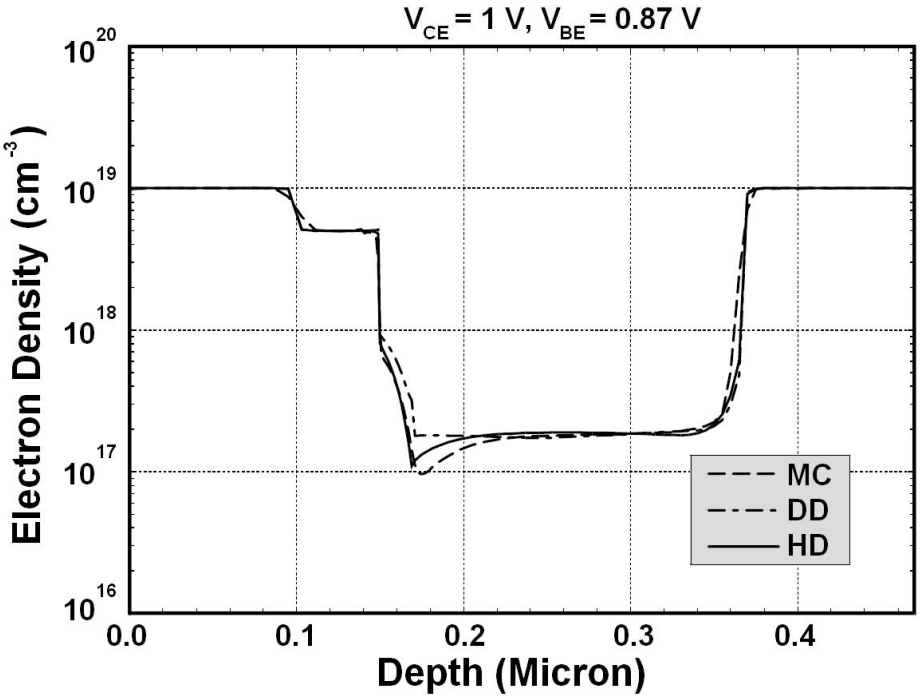

Figure 33: Vertical electron density profiles.

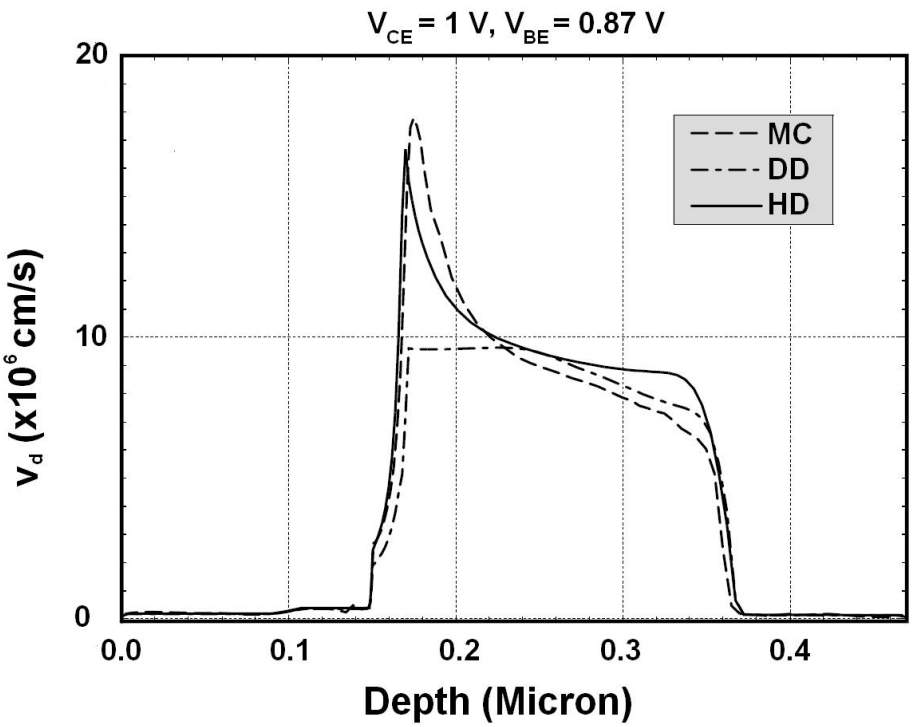

Figure 34: Vertical mean drift velocity profiles.

drift velocity resulting from 2D DD, HD, and MC simulations in steady state for $V_{BE} = 0.87$ V and $V_{CE} = 1$ V, the bias for peak cutoff frequency [51]. Moreover, Jungemann *et al.* [49] compared the electron transit times calculated by DD, HD, and MC device simulations for a SiGe HBT. The results showed good agreement between the HD and the MC model. Bartels *et al.* [50] performed comprehensive HD simulations (*dc* and *ac*) with an industrial SiGe HBT. The results showed good agreement with experimental data. The simulated *dc*/*ac* results were also verified with measured data for the HD model for this study and Figure 35 shows the simulated forward-mode Gummel characteristic compared to the measurement. The simulations and measurements were performed at the same lattice temperature (ambient temperature). The agreements of both the collector current and the base current are perfect. Figure 36 compares the simulated cutoff frequency with the measured data. Although the simulated peak f_T is underestimated, the simulation captured the curve shape and the other regions of the curve agree with the measurement very well. Both showed good agreement between the simulated data and the measured data demonstrate once again that the HD model is accurate, efficient and reliable for SiGe HBT simulations.

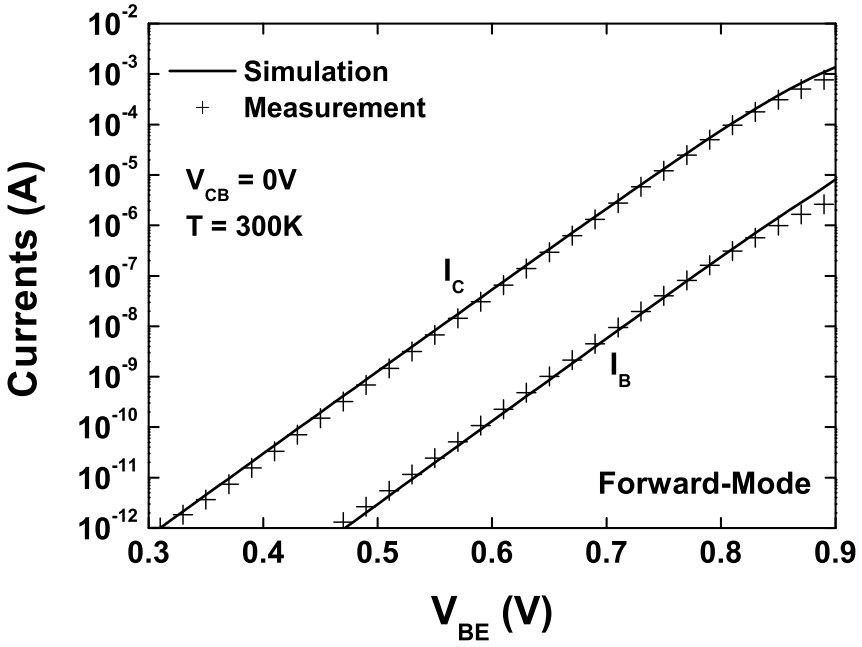

Figure 35: The comparison between the simulated and measured forward-mode Gummel characteristics of 7HP SiGe HBT with $V_{CB} = 0$ V at 300 K.

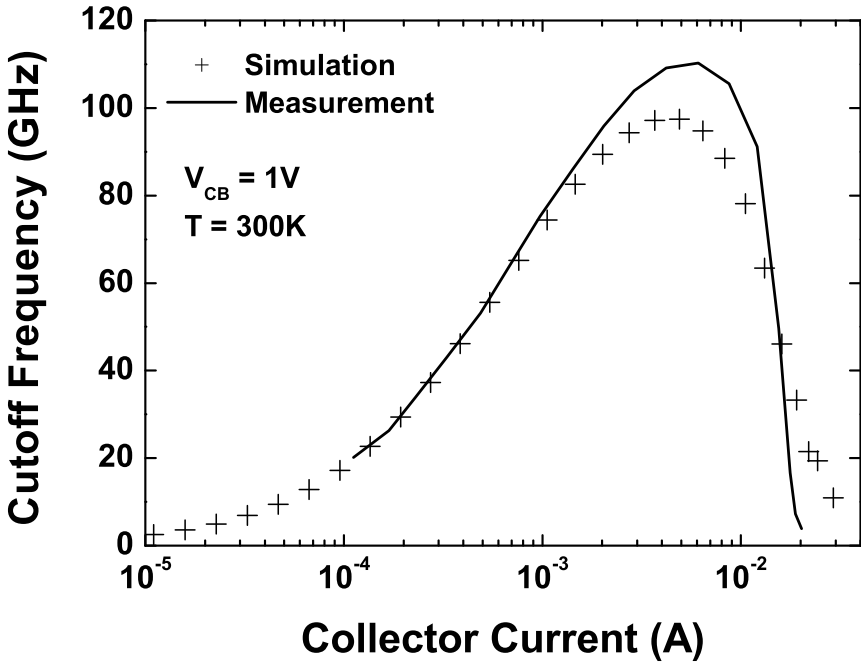

Figure 36: The comparison between the simulated cutoff frequency of 7HP SiGe HBT and the measured one with $V_{CB} = 1$ V at 300 K.

3.3 Lucky-Electron Gate Current Model

Impact ionization is one of the foremost concerns for device simulations since avalanche generation plays an increasingly important role in modern devices. By scaling down the device geometry while keeping the supply voltage constant, the electrical field increases so impact ionization plays an important role in device degradation due to hot-carrier effects that leading to leakage currents, such as gate current leakage, substrate current, base current leakage, etc.

The "lucky-electron" model is one of the impact ionization models that has been successfully used in impact ionization simulations [52]-[58]. The lucky-electron concept was proposed by Shockley [59] in 1961. In his work, Shockley assumed that an electron gains energy from the electric field without a collision. In a collision occurs, the electron loses all its energy and begins again with zero energy. The total loss of energy during the scattering process is justified with the random direction of the electron's velocity after the collision. The probability of this event is $e^{-d/\lambda}$, where λ is the hot carrier's mean free path, and d is the distance that particles will travel.

Impact ionization models can be divided into two types, namely local and non-local models. Local impact ionization models assume the ionization probability is a function only of the local value of the electric field [60]. However, impact ionization is an inherent non-local process in modern devices. After an impact ionization event, a carrier needs to travel a certain distance before it can gain sufficient energy from the electric field to have a non negligible impact ionization probability. This distance can only be ignored if it is small compared to the thickness of the multiplication region. Therefore, a non-local impact ionization model was chosen in this work.

There are two generation models presented in [58], the hard threshold model and the soft threshold model. With the hard threshold model, a constant energy scattering rate is used, while in the soft threshold model, energy scattering rate is a function of the energy difference above the threshold [39]. The work in [58] demonstrated much better accuracy using soft-threshold model. Furthermore, it has been demonstrated that the nonlocal soft-threshold lucky-electron (NSLE) model, combined with the HD model, offered a predictive modeling capability for impact ionization [52], as shown in Figures 37 and 38. The researchers compared the NSLE model and full-band Monte-Carlo (FB-MC) model in terms of the quantum yield and the substrate current simulations. The

results agree very well. Therefore, the NSLE model is used here to depict the impact ionization process in the MMS.

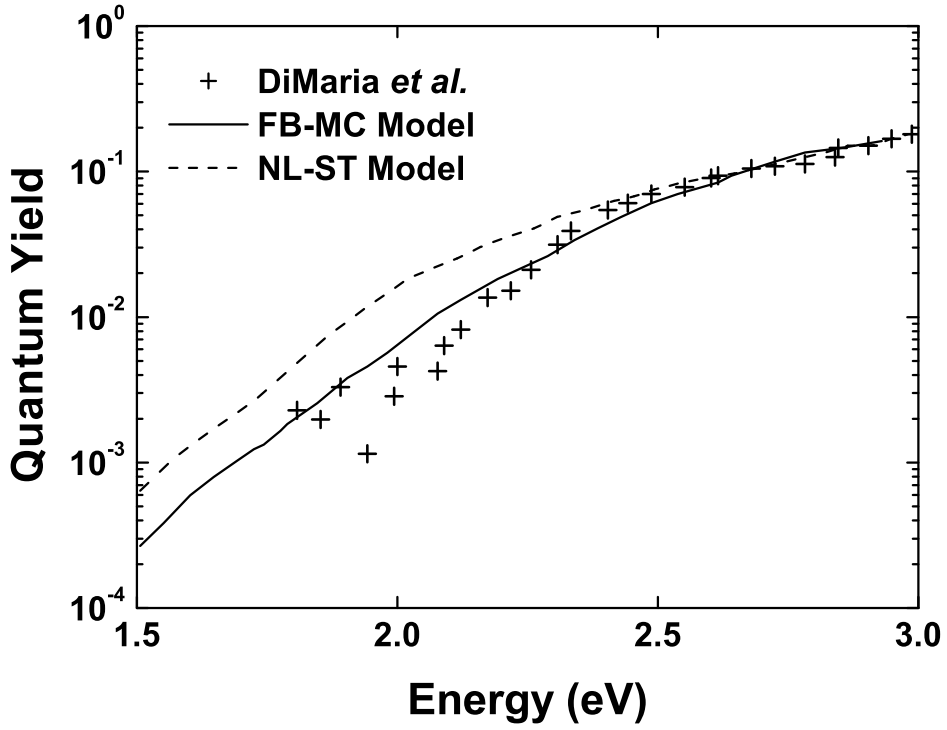

Figure 37: Quantum yield versus injection energy for bulk silicon [55], and results of the FB-MC model and NSLE model.

Figure 39 shows the hypothetical trajectories of stress-induced electrons in the SiGe HBT based on the NSLE model. Electrons are injected from the emitter. In the CB junction, they become "hot" electrons due to the high field associated with V_{CB}, and then scatter because of the impact ionization effect. Electron (a) does not carry enough energy to create a trap at the EB spacer oxide interface, though it can reach the region. The path of electron (c) does not take it to the EB spacer, so the electron (c) cannot reach the oxide interface to create the trap, no matter how large an energy it carries. Electron (b) is the "lucky" electron that is sufficiently energetic to create a trap at the EB spacer oxide surface. The lucky-electron model calculates the probabilities for such scattering events to occur, resulting in current going through the insulator, which in SiGe HBT technology means the EB spacer and STI dielectrics.

In MEDICI simulations, the gate current module is turned on to analyze the leakage current. The

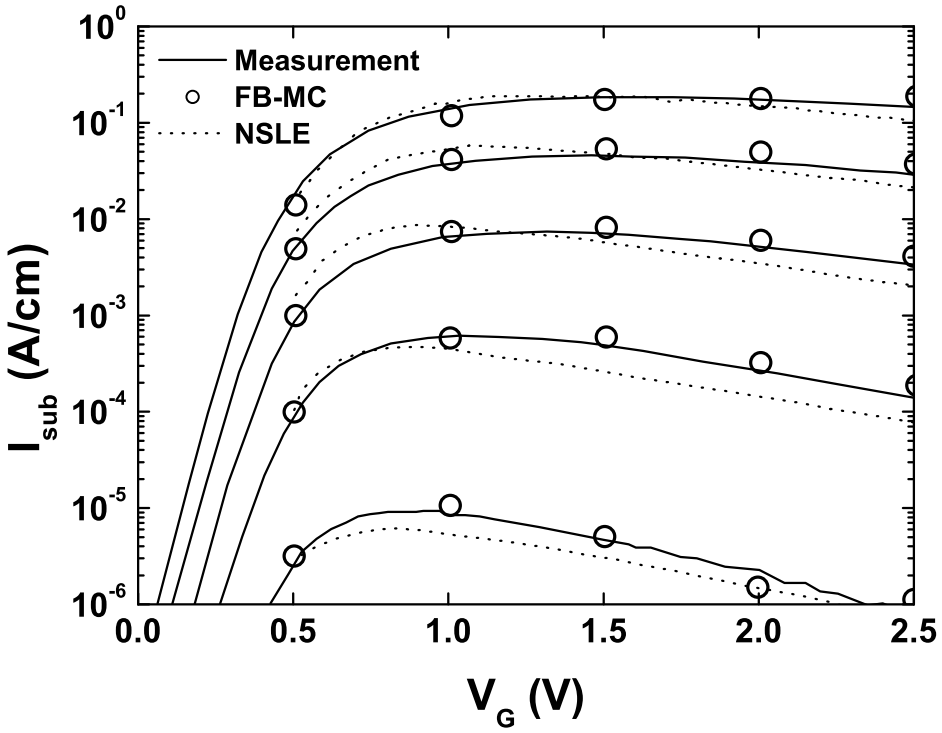

Figure 38: Substrate current versus gate voltage for 0.16 μm-NMOSFET (V_{drain} = 1.5 V, 2.0 V, 2.5 V, 3.0 V, and 3.5 V), FB-MC with surface roughness scattering and NSLE model.

gate current calculation is based on the work in [56]. The model is then referred to as the "lucky-electron gate current (LEGC) model," as shown in Figure 40. The model calculates probabilities for certain scattering events to occur that result in current being injected into the gate. The total gate current is [39]:

$$I_{gate} = \int\int \Gamma_n(x, y) \left| J_n(x, y) \right| dxdy + \int\int \Gamma_p(x, y) \left| J_p(x, y) \right| dxdy \tag{20}$$

where J_n and J_p are the electron and hole current densities. Γ_n and Γ_p are the probabilities per unit length (in the direction of current flow) that electrons or holes, respectively, in the vicinity of the point (x,y) will be injected into the gate. Γ_n and Γ_p can be expressed as the following:

$$\Gamma_{n,p} = P_{\phi_{n,p}} P_{semi_{n,p}} P_{insulator_{n,p}} / \lambda_{n,p} \tag{21}$$

where $P_{\phi_{n,p}}$ is the probability that an electron/hole will acquire sufficient kinetic energy to surmount the insulator potential barrier ϕ, and retain the appropriate momentum after re-direction. $P_{semi_{n,p}}$ is the probability that an electron/hole will not be scattered in the semiconductor before reaching

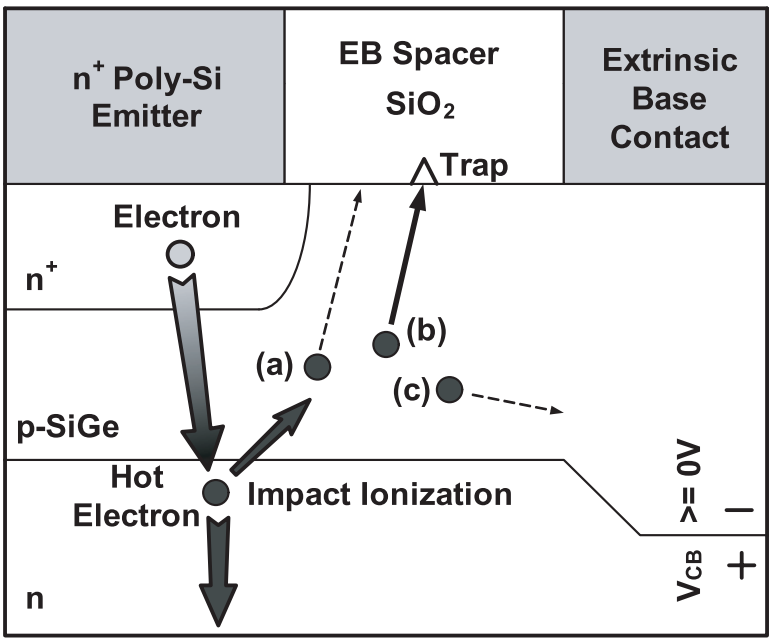

Figure 39: Electron trajectories in the SiGe HBT under mixed-mode stress: (a) Impact Ionization-Induced Hot Electron (IIIHE) reaches the oxide interface without enough energy to produce damage; (b) Lucky-Electron: IIIHE with sufficient energy creates an interface trap at the EB oxide interface; (c) IIIHE scatters away from oxide interface without doing damage.

the interface. $P_{insulator_{n,p}}$ is the probability that an electron/hole will not be scattered in the insulator between the interface and the potential barrier peak. $\lambda_{n,p}$ represent to the hot electron/hole scattering mean free path lengths.

Consider once again the scenario shown in Figure 39. After gaining enough kinetic energy and being directed in the appropriate direction, the electron must not be scattered again (i.e., lose its energy) before reaching the peak of the potential barrier in the insulator. Here, the issue is the damage at the insulator interfaces. As 9.2 nm is used as the scattering mean free path length (randomly moving) for hot electrons in the simulations, the EB spacer and the STI edge are both within this mean free path length of the hot carriers generated in the CB junction by impact ionization.

Based on the LEGC model, the Si-SiO_2 interface trap production is correlated with the hot-carrier injection current density [61]. Hence, the product of the local electron current density and the probability indicates the likelihood of these electrons reaching the oxide interface with a kinetic energy higher than the interface trap creation activation energy. Here, an activation energy of 2.4 eV [61] is applied for the interface trap creation process. The trap creation rate is proportional

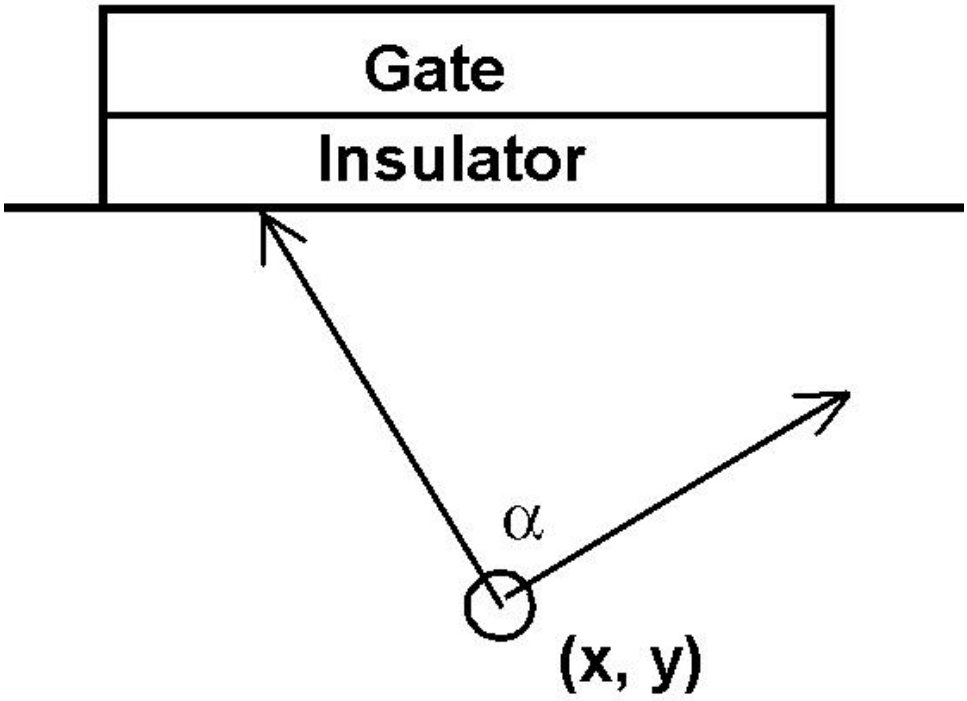

Figure 40: Lucky-electron gate current model.

to the integration of the local hot electron injection current density that is injected into the interface the collector-base voltage in MMS provides the hot electron with enough energy to maintain both the impact ionization rate and the damage activation energy.

3.4 Results and Discussion

To gain a deeper insight into the mixed-mode damage physics, the hot carrier injection current was simulated under MMS conditions by fully-calibrated isothermal 2D MEDICI simulations. The local carrier temperatures (electron and hole) were calculated using the energy balance equations. The gate current analysis module was invoked, together with the nonlocal soft-threshold lucky-electron model [58].

Figure 41 shows the simulated distribution of the local HE injection current under MMS conditions, the same as in the measurement setups, for the 7HP SiGe HBT. For both the emitter-base spacer and shallow trench damage regions, the injection current density is clearly present and dominated by hot electrons, which is consistent with the data shown in Figures 6 and 7. Hot holes exist but in smaller numbers, and can thus be neglected. Recently, Vanhoucke *et. al.* [38] suggested that

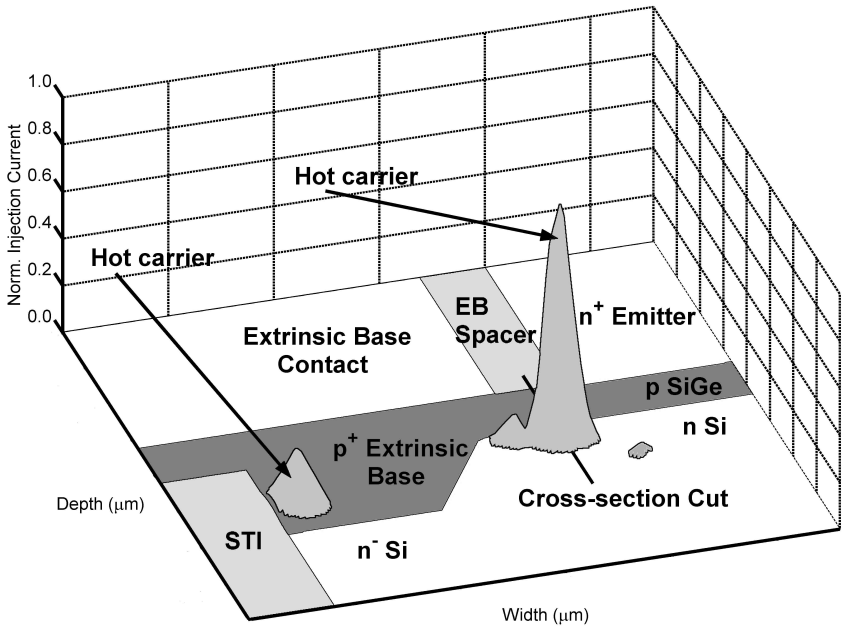

Figure 41: Simulated distribution of the local hot carrier injection current (J_E = 35 mA/μm^2, V_{CB} = 3.0 V). The peak injection currents are located at the emitter-base spacer and the shallow trench edge.

trap generation at EB spacer is caused by hot holes using 1D full-band Monte-Carlo method. This might be due to the different damage region in the damage spectrum. The stress conditions used in [38] are located at the region I—hump region. As shown in Section 2.3, it is obviously that the region I has the different damage mechanism from the region III—this work.

Simulations were also used to assess the impact of stress using variable V_{CB}. As shown in Figure 42, decreasing V_{CB} effectively decreases not only the impact ionization rate that decreases the density of carriers in the CB junction, but also the average kinetic energy of the hot carriers that decreases the probability of "lucky" electrons. Therefore, the damage at the Si-SiO_2 interface is reduced, which is consistent with the data shown in Figure 9.

Figures 43, 44, and 45 show the spatial distribution of the potential, the electric field, and the generation rate with a 5% contour in the 7HP SiGe HBT, respectively. The simulated J_E and V_{CB} are same as the conditions implemented in Figure 41. As seen in Figure 43, when V_{CB} is applied, the most significant potential drop falls on the extrinsic base-collector junction, thus increasing the electric field dramatically as shown by the crowded contours in Figure 44. Figure 46 shows the magnitude of the electric field along the cross-sectional cut in Figure 41. Combined with Figure 45,

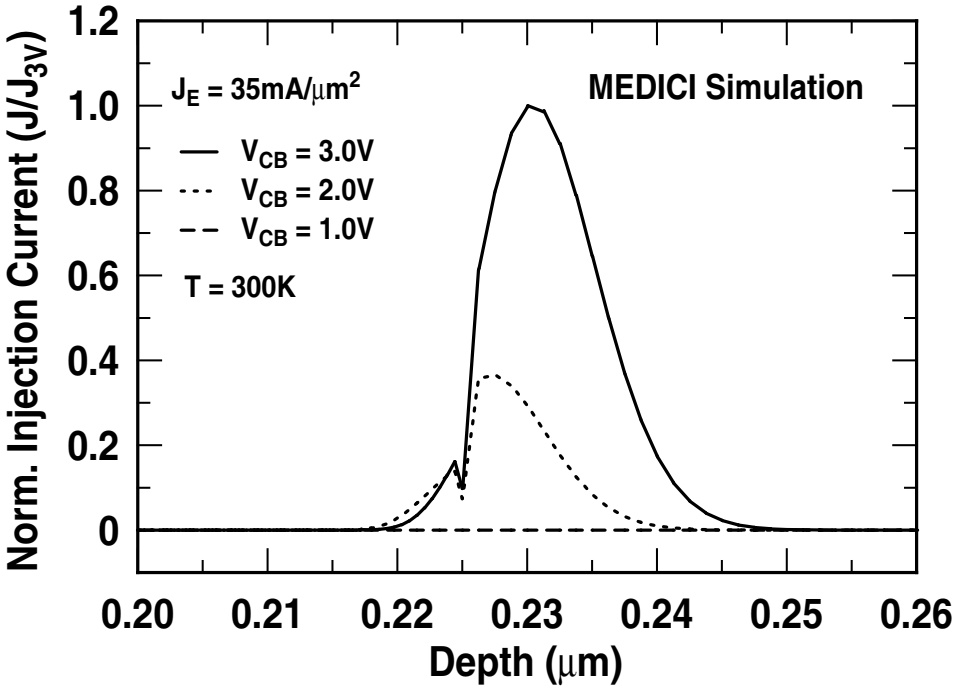

Figure 42: Simulated cross-sectional distribution of the local hot carrier injection current under different V_{CB} stressing at fixed J_E. The spatial location of the cross-sectional cut is shown in Figure 41.

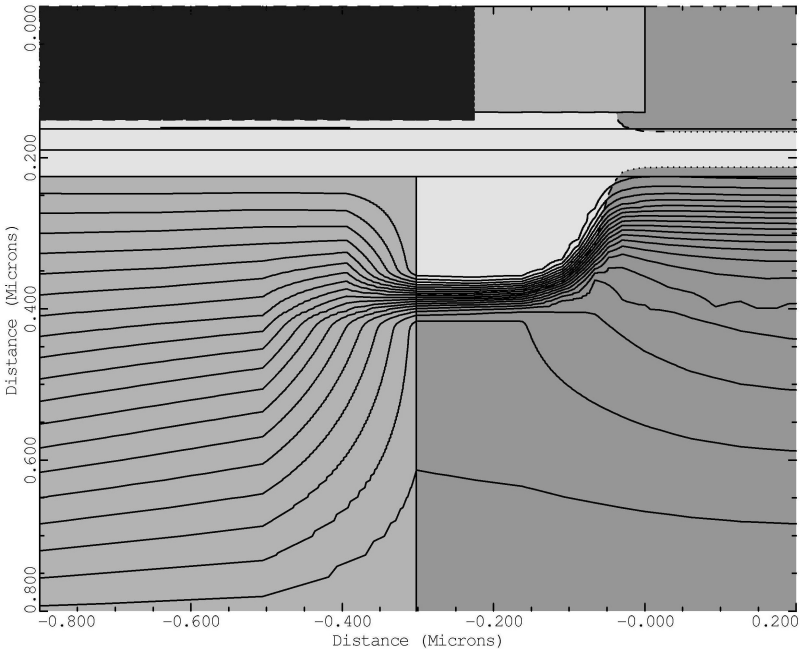

Figure 43: The 5% potential contour at 300 K.

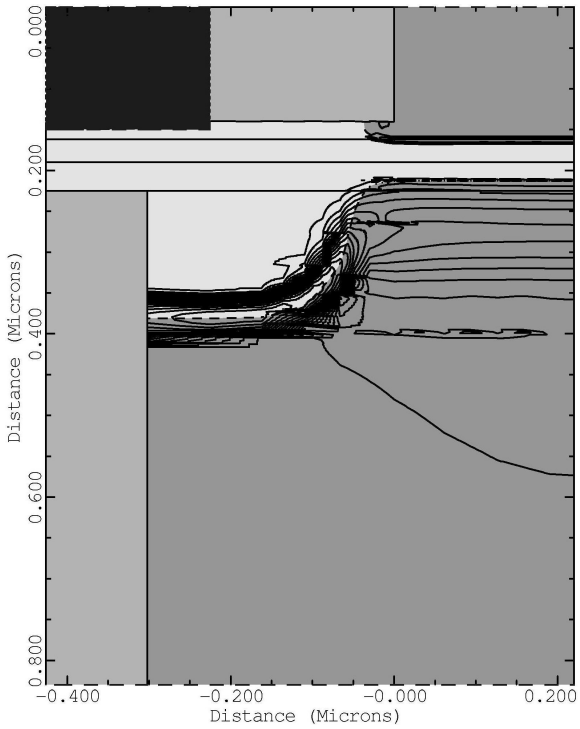

Figure 44: The 5% electric field contour at 300 K.

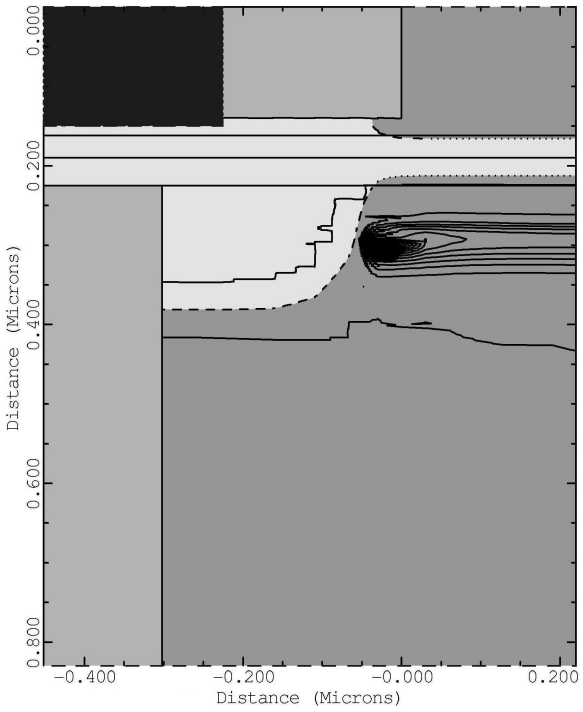

Figure 45: The 5% generation rate contour at 300 K.

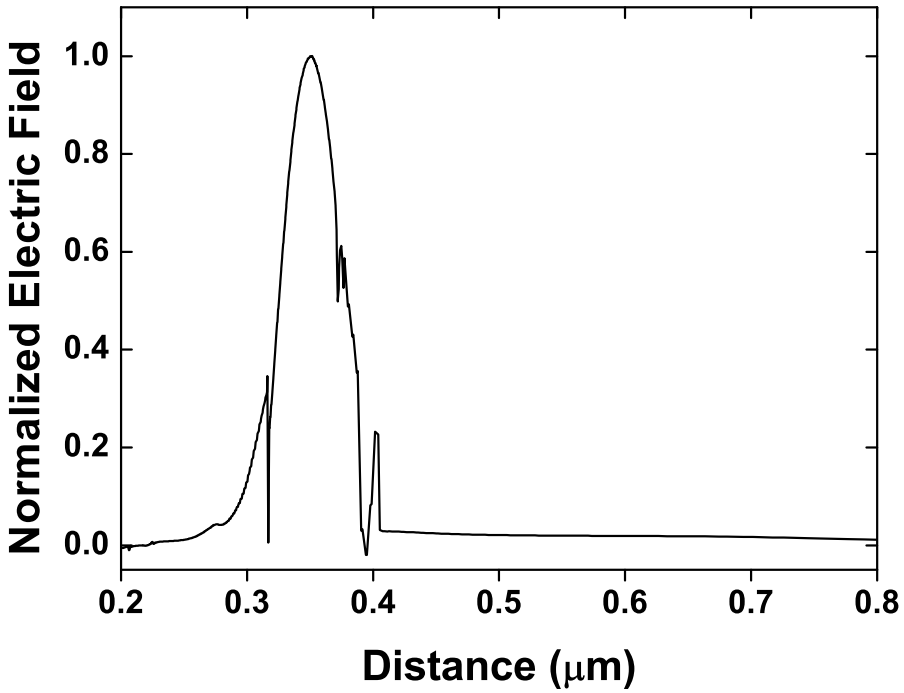

Figure 46: Simulated cross-sectional distribution of the electric field. The spatial location of cross-sectional cut is shown in Figure 41.

this shows that large numbers of electron-hole pairs are generated after the peak electric field, indicating that strong impact ionization occurs when injected electrons gain enough energy through the electric field.

When shifting the STI edge away from emitter edge, thus increasing ST-EM spacing, the simulation results in Figure 47 clearly show that the hot electron peak near the STI edge also shifts away with the same distance and with a smaller magnitude, while keeping the position of the hot electron peak underneath the EB spacer essentially unchanged. Consequently, the effective physical proximity of the location of the impact ionization moves further away from the emitter edge with smaller magnitude.

Figure 48 shows that increasing the ST-EM spacing decreases the damage production rate due to an effective repositioning of the hot carrier profile to a location further away from the emitter-base spacer, which is consistent with the data shown in Figure 12.

As shown above, the impact ionization effect during MMS is simulated. However, it is not easy to simulate the strong self-heating effect due to severe convergency issues.

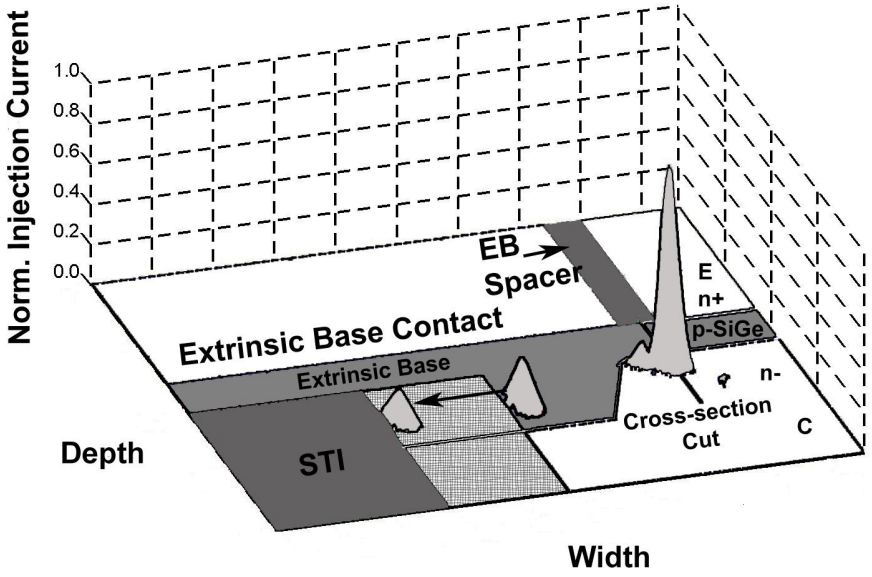

Figure 47: Hot electron profiles distribution with varying ST-EM spacing.

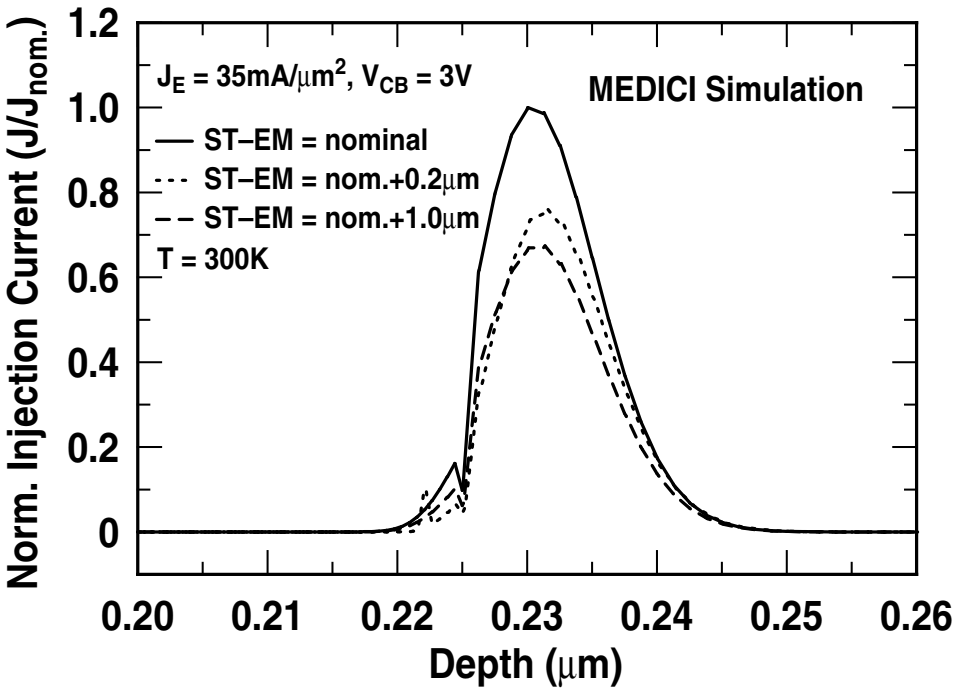

Figure 48: Simulated distribution of the local hot carrier injection current as a function of shallow trench to emitter spacing. The spatial location of the cross-sectional cut is shown in Figure 47.

3.5 Summary

In this chapter, an industry-standard device simulator, MEDICI, was used for an MMS study. First, the MEDICI simulation steps were introduced briefly, followed by the carrier transport models. Typically, DD and HD transport models are used within TCAD frameworks due to efficiency and acceptable accuracy. The HD model was compared with well-known Monte-Carlo model in Section 3.2, indicating that the HD model is still reliable even for advanced SiGe HBT simulations. Furthermore, good agreement for both the *dc* characteristics and the cutoff frequency between measurements and simulations provided support for the validation of HD model. The Lucky-electron concept was then introduced for impact ionization modeling. The gate current model based on the non-local soft threshold lucky-electron model was introduced and implemented in the MMS simulation. Finally, the simulation results were presented to provide a better understanding of the damage mechanisms involved, which were also consistent with the measurements reported in Chapter 2.

CHAPTER IV

SIGE HBT RELIABILITY ASSESSMENTS AT EXTREME TEMPERATURE

4.1 Introduction

Careful design of the bandgap in SiGe makes it possible to operate SiGe devices and circuits down to deep cryogenic temperatures (as low as 4 K), an operational domain forbidden to conventional Si bipolar technologies [63][64]. At present, cryogenic electronics represents a niche industry, with applications in high-sensitivity cooled sensors and detectors, semiconductor-superconductor hybrid systems, orbital space electronics, sub-systems for planetary missions, and instrumentation electronics [65].

One new and interesting cryogenic application involves NASA's recent presidentially-mandated refocus on Lunar exploration. The surprisingly extreme temperature conditions on the Lunar surface (as low as -230 °C in the polar shadows, and a range from -180 °C to +120 °C for Lunar night to day) precludes the use of conventional terrestrial electronics for sensing, actuation, and control. This raises serious issues for planner, since the development of modular, expandable, and reconfigurable human and robotics systems for Lunar missions clearly require electronic components and integrated packaged electronics modules that can operate robustly and reliably without external thermal control. Unmanned lunar missions necessarily combine mobility on the surface (e.g. on a Lunar rover) with sensing functions, electronics, and motor/actuators for control of the vehicle. Of particular interest is the remote electronics unit (REU) used to define intelligent electronics nodes that are capable of remote operation. Since these REUs are in principle distributed over the entire vehicle, they can't be efficiently located within protective "warm boxes." Currently, this need for protective electronic "warm boxes" critically limits attempts to create truly distributed, modular electronics systems for such applications, resulting in excessive point-to-point wiring, increased system weight and complexity, lack of modularity, and an overall reduction in system reliability.

The use of SiGe-based mixed-signal electronics capable of operating down to cryogenic temperatures has the potential to change this situation dramatically. Clearly, the requisite SiGe devices must first be proven reliable in the cryogenic environment. This chapter examines the reliability of SiGe HBTs by first showing both theoretically and experimentally the impact of temperature on SiGe HBTs, and then addressing comprehensive data and 2D MEDICI simulations at the cryogenic temperature. The last section of the chapter concludes with a consideration of the high temperature reliability issue.

4.2 The Impact of Temperature On SiGe HBTs

The bipolar transistor is a minority carrier transistor,where the currents (I_E, I_B, and I_C) are proportional to the square of the intrinsic carrier concentration square (n_i^2). n_i^2 is proportional to $e^{-E_g/kT}$, where E_g is the bandgap. E_g also has T-dependency, as described by Varshni's equation,

$$E_g(T) = E_g(0) + \frac{\alpha T^2}{T + \beta} \tag{22}$$

where $E_g(0)$, α and β are the fitting parameters. Hence, the bandgap variation will induce the current variation exponentially. E_g is also divided by the thermal energy (kT). Thus, the reduction in temperature will magnify the E_g change. The equations for β, V_A, and τ_b were given in Section 1.2; all kT items in the equations will help enhance performance at low temperature.

Current gain is clearly important for mixed-signal circuit design, and it also determines breakdown voltage (e.g. BV_{CEO} occurs when $(M - 1) \times \beta = 1$). Figure 49 shows the relationship between J_C and current gain β for different temperatures. The current gain is observed to increase with cooling, as expected. The maximum current gain at 85 K is almost 1.7 times that at room temperature, which is more than adequate for circuits at 85 K (see Figure 50).

The transit time decreases with cooling, as predicted by the theory, suggesting that the cutoff frequency f_T increases. Figure 51 shows the f_T at 162 K, 223 K, and 300 K and Figure 52 illustrates the relationships between $1/2\pi f_T$ and $1/I_C$ at the same temperatures. The extrapolated intercept at $1/I_C = 0$ can be used to determine the transit time, as f_T increases is due to decreasing transit time.

Figure 53 shows the output characteristics at 85 K and 300 K for a range of forced base currents. The data demonstrate that the output current level with the same input base current increases with

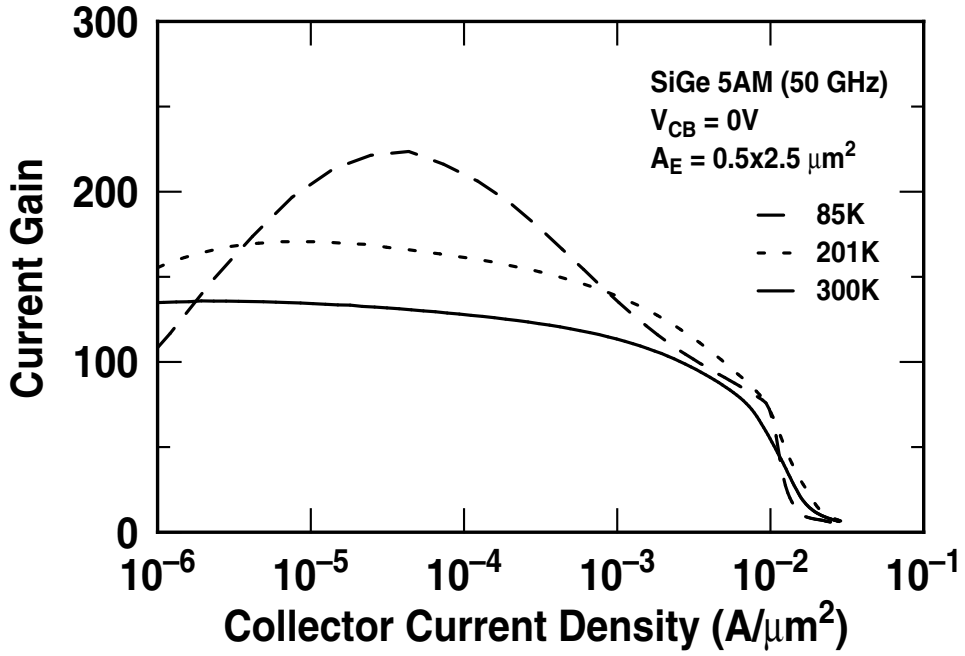

Figure 49: Current gain vs. collector current density at 85 K, 201 K, and 300 K.

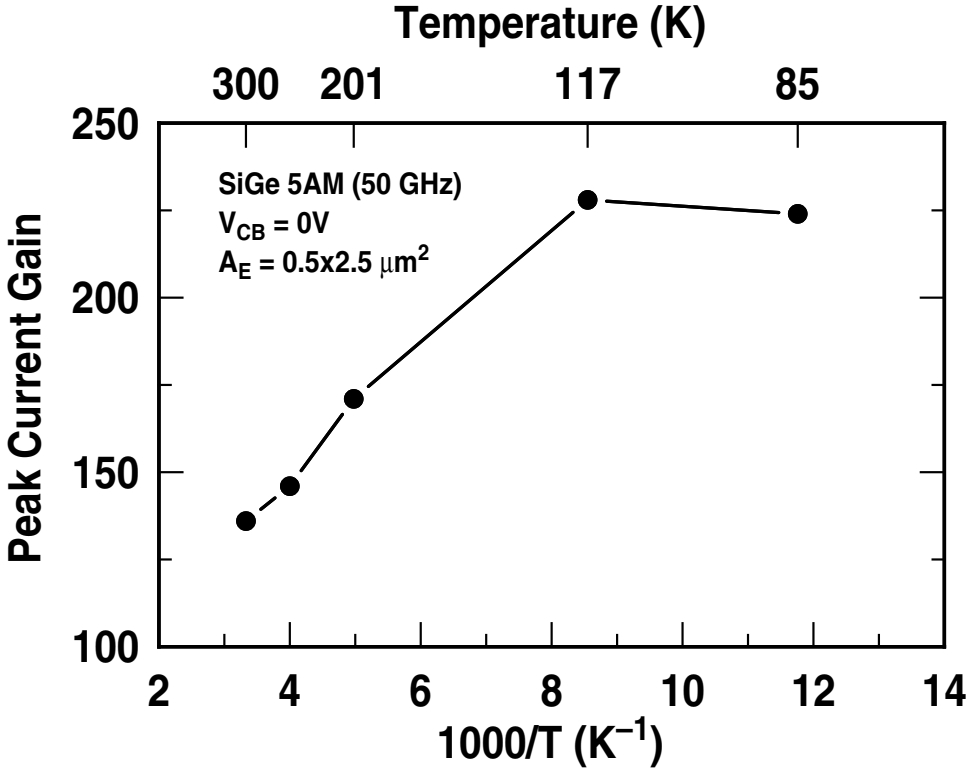

Figure 50: Maximum current gain vs. 1000 / $T_{ambient}$.

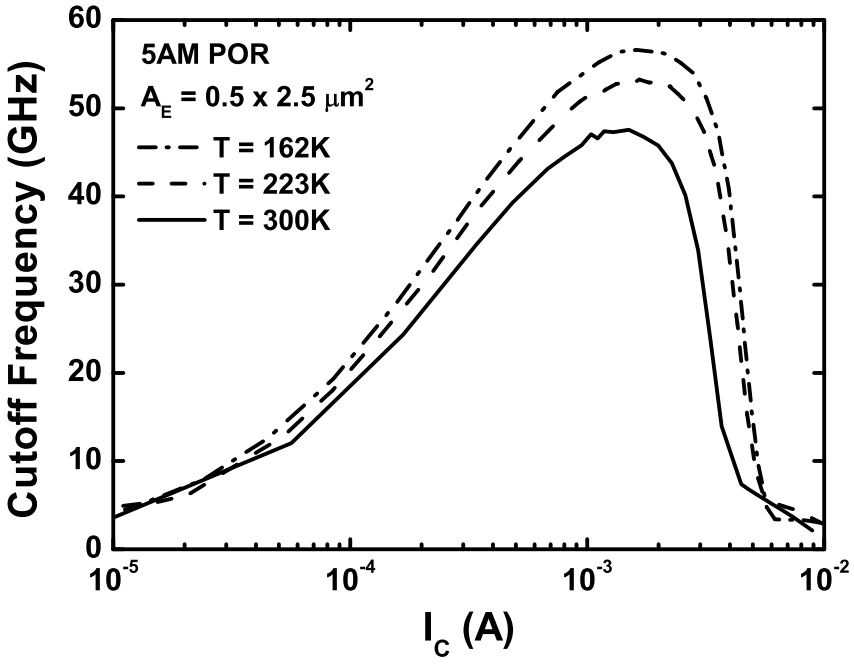

Figure 51: Cutoff frequency versus I_C at 162 K, 223 K and 300 K.

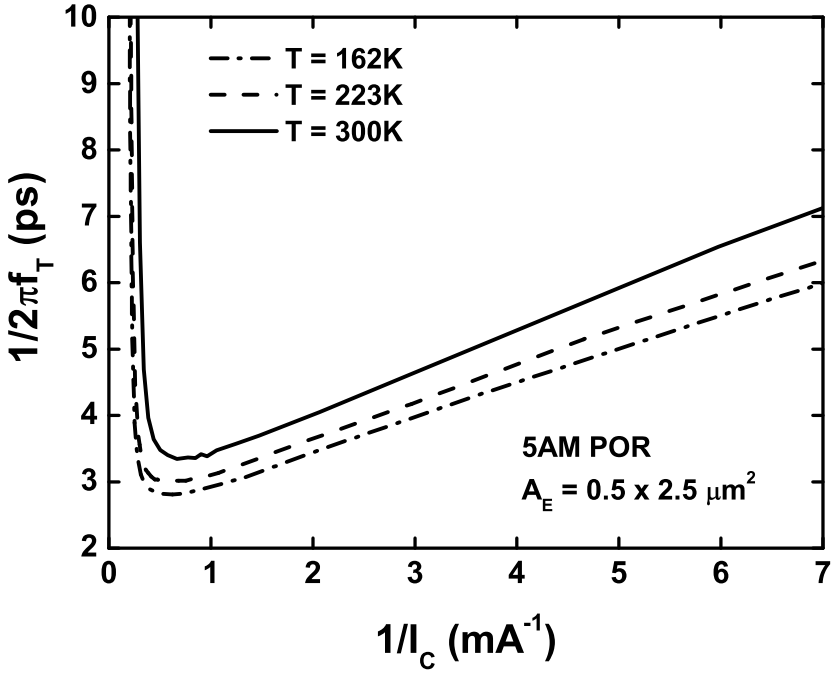

Figure 52: $1/2\pi f_T$ versus $1/I_C$ at 162 K, 223 K and 300 K. The extrapolated intercept at $1/I_C = 0$ can be used to determine the transit time.

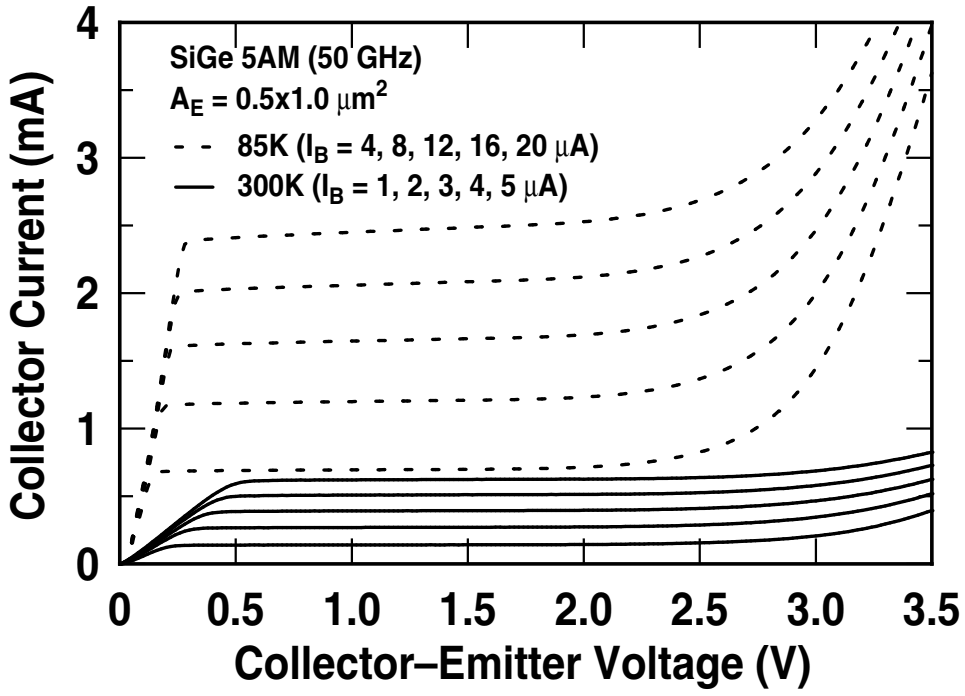

Figure 53: CE-forced I_B output characteristics at 300 K and 85 K.

higher current gains at the lower temperature and the dynamic swing capability of the device is slightly compressed under cryogenic conditions indicating a modest decrease in breakdown voltage.

Figure 54 shows the extracted avalanche current multiplication factor $M - 1$ for three different temperatures—85 K, 195 K, and 300 K, by forced-I_E measurements [66]. $M - 1$ increases slowly with cooling, as expected, since the carrier mean free path lengths (and hence average energy) increase with cooling.

As is well known, the thermal resistance at cryogenic temperatures is smaller than at room temperature, which indicates the improvement of the self-heating effect during mixed-mode stressing, as discussed in Chapter 2. Using the described technique in [8], the device self-heating temperature ΔT was measured at 90 K and 298 K. Figure 55 demonstrates that ΔT is linearly dependent on the dissipated power even at cryogenic temperatures, as expected, indicating that the extracted thermal resistances are approximately constant at each temperature — 4,640 K/W at 298 K, and 2,400 K/W at 90 K. The latter value is almost half that at 298 K, a significant improvement, implying mitigated self-heating effect and damage threshold shift (see Figure 26) at cryogenic temperatures.

Avalanche-induced breakdown and related bias instabilities are also of practical concern for

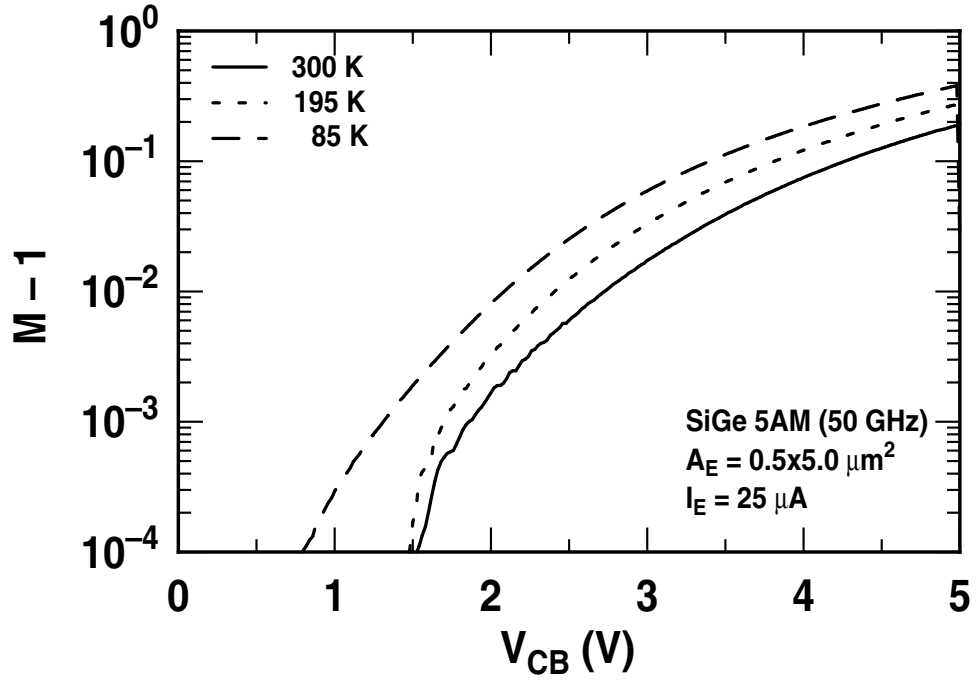

Figure 54: Avalanche multiplication factor for SiGe HBTs at 85 K, 195 K, and 300 K.

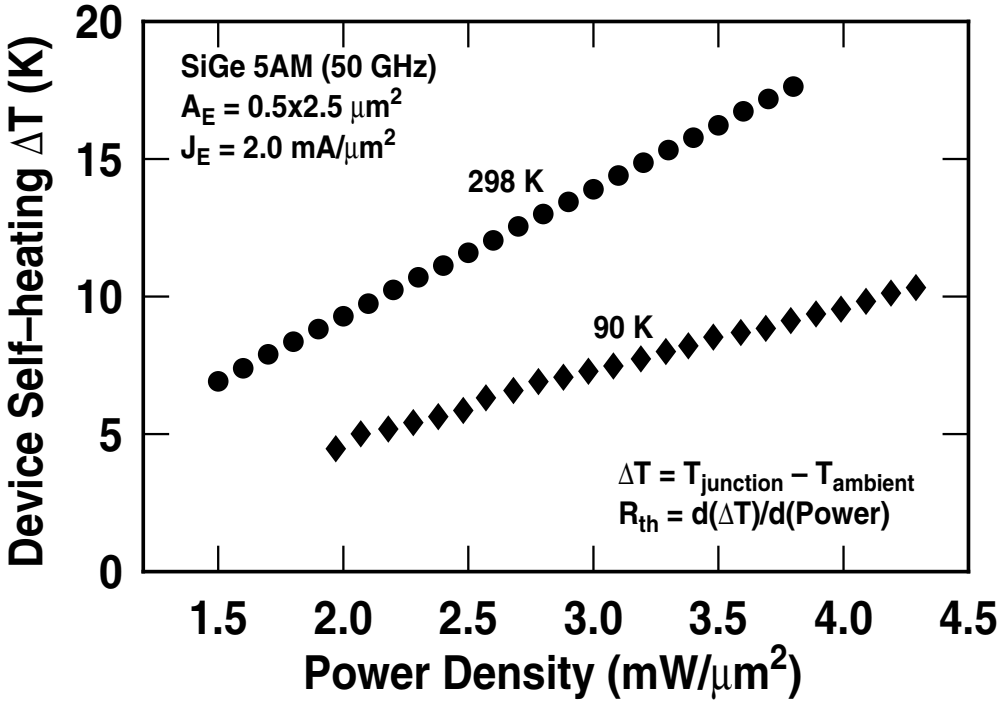

Figure 55: Device self-heating temperature ΔT vs. dissipated power density at 90 K and 298 K.

circuit designers. Unfortunately, unlike the current gain, the breakdown voltage deteriorates with decreasing temperature. Grens [62] compared the measured BV_{CBO} (best case for circuits), BV_{CEO} (worst case for circuits), and the critical V_{CB} before the onset of pinch-in induced bias instabilities under forced current drive ($V_{CB,crit}$)—a practical upper bound bias point for many circuits [67], as illustrated in Figure 56. All of these voltages decrease with temperature. Due to its dependence on

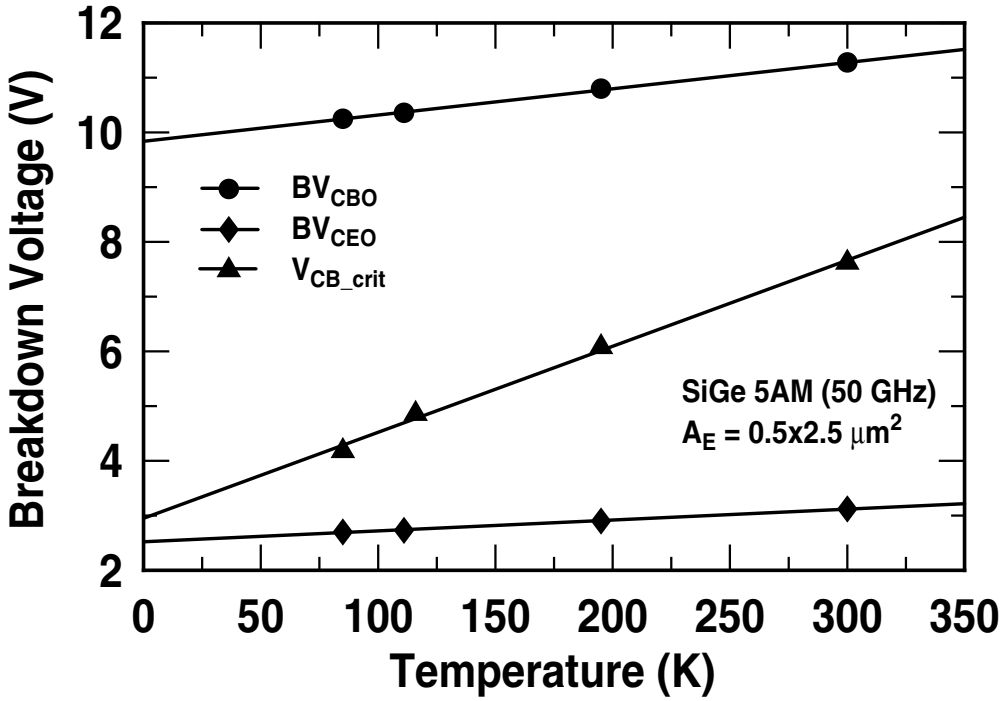

Figure 56: Breakdown voltages as a function of temperature.

both $M-1$ and parasitic r_B, which increases slightly with cooling due to carrier freeze-out, $V_{CB,crit}$ has the fastest rate of decrease across temperatures, with almost a 50% reduction from 300 K to 85 K, which is clearly of concern for circuits biased above BV_{CEO}. Generally, however, these decreases in operating voltages with cooling are not especially alarming, so optimization of the Ge and doping profiles to mitigate these decreases should be easily accomplished if necessary.

4.3 Mixed-Mode Stress At Cryogenic Temperature

The SiGe HBTs investigated here were commercially-available, fully-integrated, first-generation SiGe HBT BiCMOS devices (IBM SiGe 5AM) [68][69]. Most electronics components for potential Lunar applications do not require excessively high speeds and thus first-generation SiGe technologies, which are also less expensive, are more than adequate, particularly since their device performance metrics are expected to improve with cooling. The low-breakdown voltage SiGe HBT examined here has a 50 GHz peak f_T at a collector current density of 2 mA/μm^2 at 300 K, and around 4 mA/μm^2 at 85 K. During the stress test, the device temperature was precisely controlled to within ±0.1K using a Blanz model 102 liquid nitrogen probe station with on-wafer probing capability.

4.3.1 Experiment Results

Typical forward-mode and inverse-mode Gummel characteristics, prior to and following 1000 seconds of applied MMS at J_E = 30 mA/μm^2 and V_{CB} = 3.0 V, are presented at 300 K and 85 K in Figures 57 and 58, for stress applied at 300 K and 85 K, respectively. These SiGe HBTs exhibit

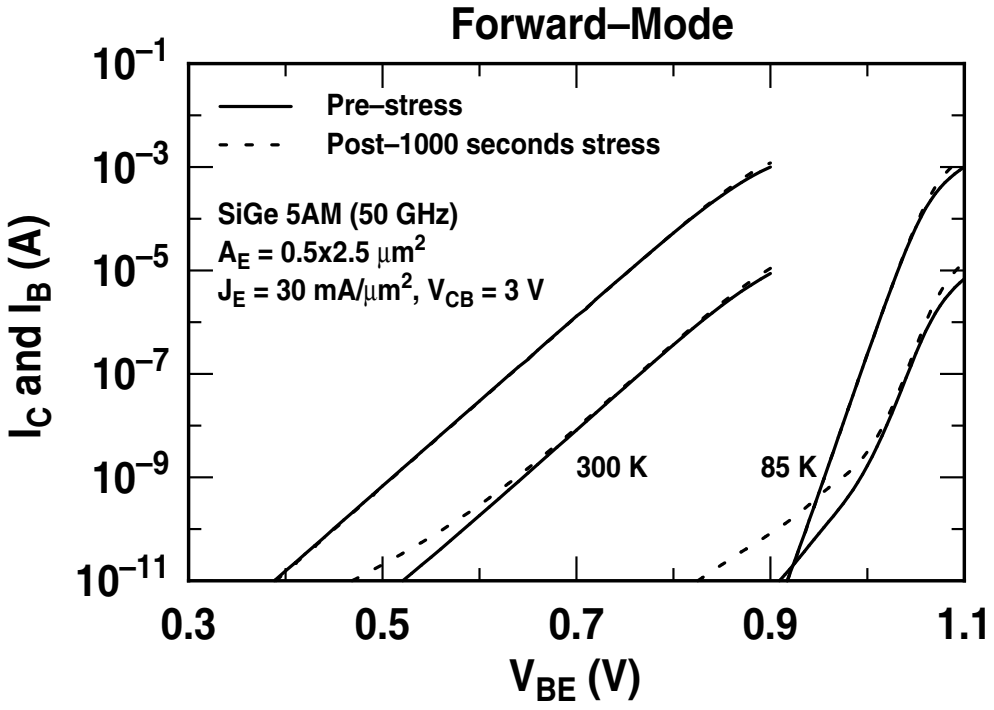

Figure 57: Forward-mode Gummel characteristics at 300 K and 85 K both before and after the mixed-mode stress with J_E = 30 mA/μm^2 and V_{CB} = 3.0 V.

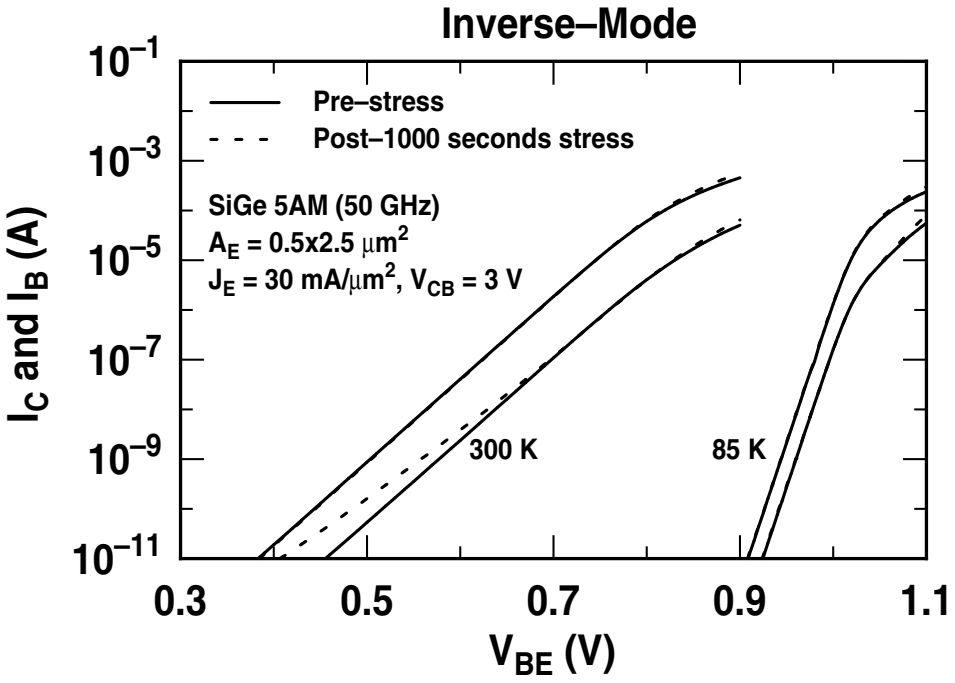

Figure 58: Inverse-mode Gummel characteristics at 300 K and 85 K both before and after mixed-mode stress with $J_E = 30$ mA/μm^2 and $V_{CB} = 3.0$ V.

adequate current gain over many orders of magnitude, improved transconductance, and excellent output current drive at 85 K compared to 300 K, clearly good news for cryogenic circuit designer. The DUTs are also optimized for cryogenic applications. The heterojunction barrier effect is not serious in this device at 85 K due to the use of a retrograded Ge profile and high collector doping [1]. As expected, the applied MMS at 300 K results in an increase in the non-ideal base current at low injection. The ideality factor of the post-stress base current is approximately 2 at 300 K. However, at 85 K the ideality factor shifts from 2.6 to 5.03 for pre vs. post stress at low injection. This phenomena is similar as that induced by reverse-EB stress at 77 K [70]. As discussed in previous chapters, in MMS the hot electrons are injected into the EB spacer oxide, thereby producing generation-recombination (G/R) centers and hence the resulting "non-ideal" base current observed in both forward-mode and inverse-mode Gummel characteristics. When the temperature decreases, however, the Shockley-Read-Hall (SRH) process which dominates EB recombination at 300 K can be assisted by the more weakly temperature dependent Poole-Frenkel field-enhanced tunneling in the high-field EB space-charge-region (SCR), resulting in an ideality factor greater than 2. There is

clear evidence for this in the pre-stress base current non-ideality at 85 K.

The damage phenomena observed in the inverse-mode Gummel data, which is sensitive to damage in the physical CB junction and especially at the STI edge, presented in Figure 58 is quite interesting. The collector current and base currents remained essentially unchanged during the stress applied at 85 K, indicating some self-mitigation of the STI edge damage mode. If, however, the devices are first stressed at 300 K and then re-measured at 85 K, or re-measured at 300 K after the stress is completed at 85 K, a conventional stress-induced SRH recombination current component in base current is observed. Clearly, in the STI edge damage process, stress path (and history) matters, which is itself clearly a reliability issue. It should be noted that however it is stressed, inverse mode damage is always minimal. This stress-path effect is due to the current spreading at different temperatures, as confirmed by the simulation described in the next section.

The DUTs were also stressed at 85 K under the same stress conditions as those used at 300 K, which is consistent with the way 300 K and 85 K circuits would likely be designed with the same operating bias voltages and currents. To help understand the damage kinetics in MMS, during the 85 K stress procedure, the stress measurements were paused at 1, 10, 100, and 1,000 seconds. At each stress-pause, the ambient temperature was raised to 300 K to record the Gummel characteristics, then the device was returned to 85 K to continue the stress test. Once the chuck temperature was stable at 85 K, the Gummel characteristics were recorded again before proceeding to the next pause-point. The resulting Gummels correspond closely with the Gummels measured before raising the chuck temperature to 300 K, suggesting that no thermal anneal occurred during the rapid temperature variation. Figure 59 compares the normalized excess base current at $V_{BE} = 0.7$ V (300 K) for the 300 K stress and the 85 K stress. The results are clearly different, suggesting fundamentally different damage kinetics. The base current of the device stressed at 300 K exhibits an initial increase followed by a subsequent decrease, while the base current of the device stressed at 85 K shows an increase in damage with time, albeit with a smaller magnitude. It is well-accepted that the decrease in excess I_B is due to a debiasing effect and stress-induced generation of traps in the emitter poly/mono silicon interfacial oxide layer [20].

The different degradation patterns for the stress tests at 300 K and 85 K also imply that cryogenic stress changes the lifetime of the device, and in fact the effective lifetime at 85 K is longer than that

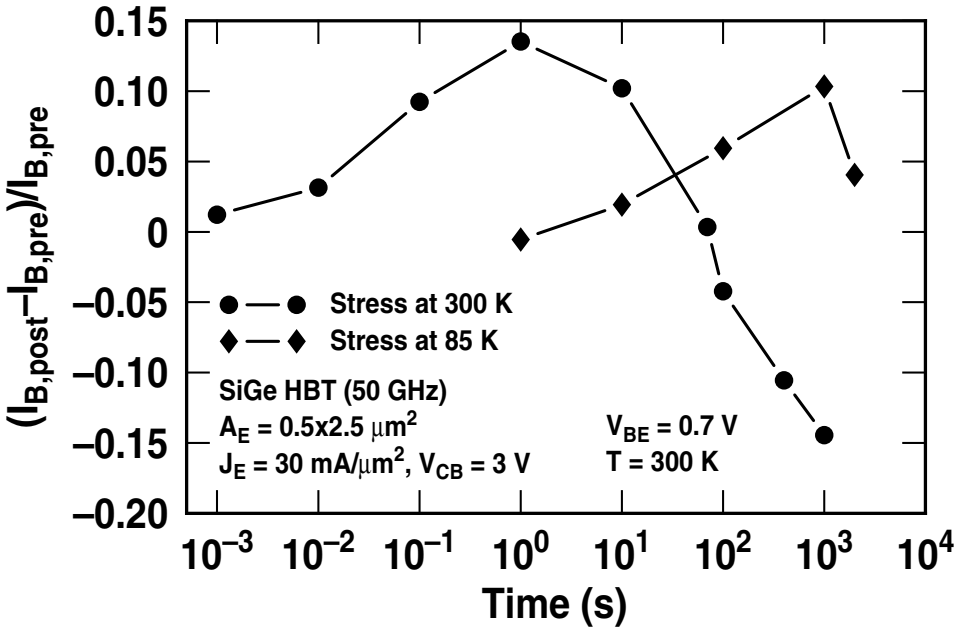

Figure 59: The normalized base current vs. stress time at a fixed V_{BE} of 0.7 V.

at 300 K (see Section 4.3.3). MMS was also applied at up to 5,000 seconds under normal circuit operating conditions (J_E = 2 mA/μm^2—the current density at peak f_T) and V_{CB} = 3.0 V at 85 K. No significant degradation was observed, which bodes well for the reliability of the device under normal circuit conditions at cryogenic temperatures.

Low-frequency noise is one of the most important tools used to investigate trap behaviors. As reported in [29], the noise power spectrum density S_{I_B} has $1/T$ dependence. Figure 60 shows the low-frequency noise power spectrum of the device at 85 K and 300 K before MMS. The noise bias conditions are I_B = 1 μA and V_{CB} = 0 V. Both curves follow a $1/f$ shape in the frequency domain, but the noise magnitude at 85 K is clearly larger than at 300 K. Figure 61 shows S_{I_B} at 10 Hz at 300 K and 85 K, for both pre- and post-1000-second stress. At 300 K, S_{I_B} for both pre-stress and post-stress are proportional to $I_B^{1.96}$ and $I_B^{1.83}$ respectively. At 85 K, S_{I_B} for pre-stress is proportional to $I_B^{2.07}$, while it is $I_B^{2.25}$ for post-stress. All fitting lines are close to I_B^2, that is, emitter area-dependent. This implies that the $1/f$ noise is dominated by the interfacial oxide in emitter poly/mono-silicon interface (area) at both room temperature and cryogenic temperatures.

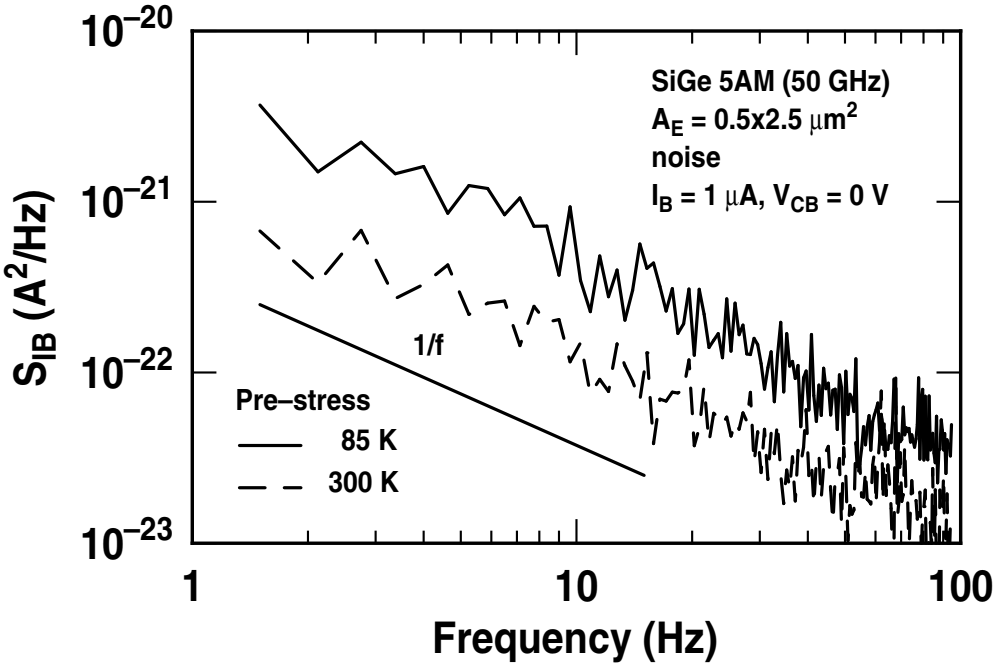

Figure 60: Pre-stress $1/f$ noise comparison at 85 K and 300 K.

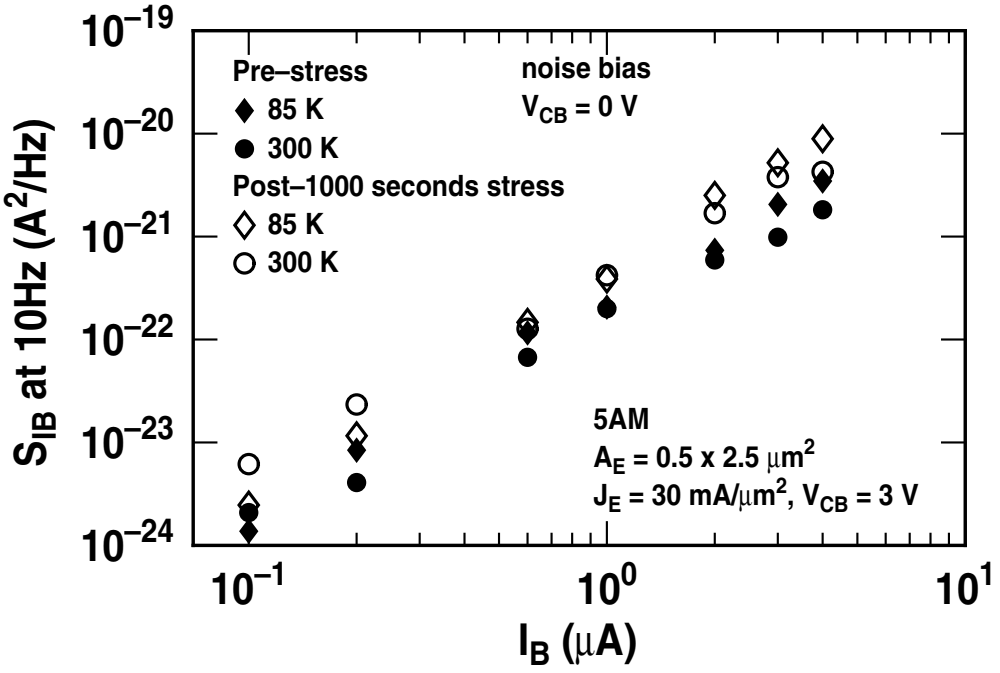

Figure 61: Noise degradation as a function of base bias current for pre- and post-1000-second stress at 300 K and 85 K.

4.3.2 2D Simulations

2D calibrated MEDICI simulations were implemented in the cryogenic reliability study. To explain the less STI edge damage at 85 K, current contours at both temperatures were simulated, as shown in Figures 62 and 63. It is clear that the current spreading effect is significantly suppressed

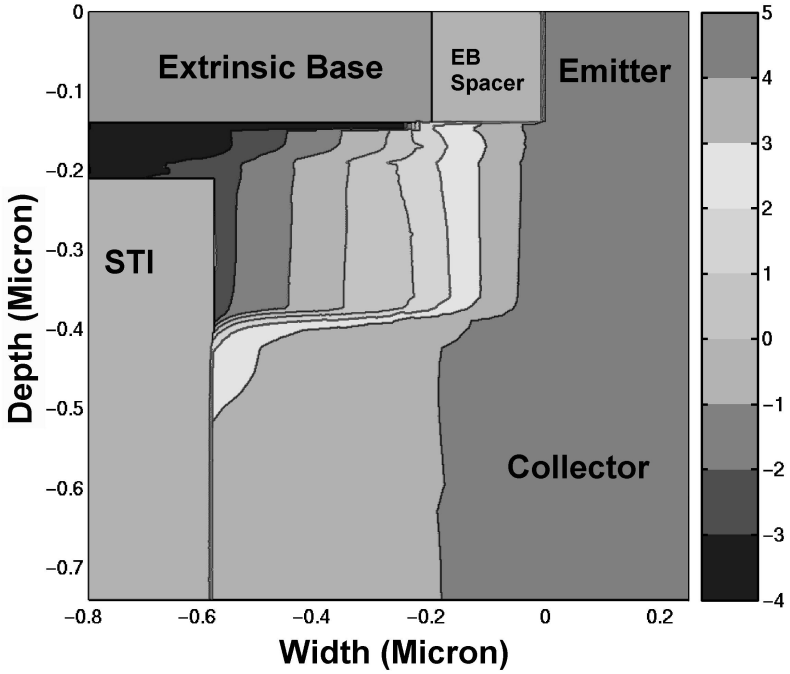

Figure 62: The current contours for 50 GHz SiGe HBTs (5AM) at 300 K.

at cryogenic temperatures. At 300 K, the current level near STI edge is 10-100 pA/μm^2, while it is 1-10 pA/μm^2 at 85 K. Although the scattering mean free path of the hot electrons increases at lower temperatures, thus raising the damage probability predicted by the lucky-electron gate current model, the total number of injection carriers decreases due to the lower current level (see Section 3.3). Thus, fewer traps are produced at STI edge.

Figures 64 and 65 simulate the current contour under inverse-mode conditions, where the emitter and collector are switched when probing, with $I_C = 0.1$ nA and $V_{CB} = 0$ V at both temperatures. Again, the current spreading effect is suppressed at lower temperatures. That means that even though there are traps at STI edge, less current flows through this surface. Thus, no significant leakage current is observed, or the pre- and post-stress inverse Gummels also correspond closely (see Figure 58).

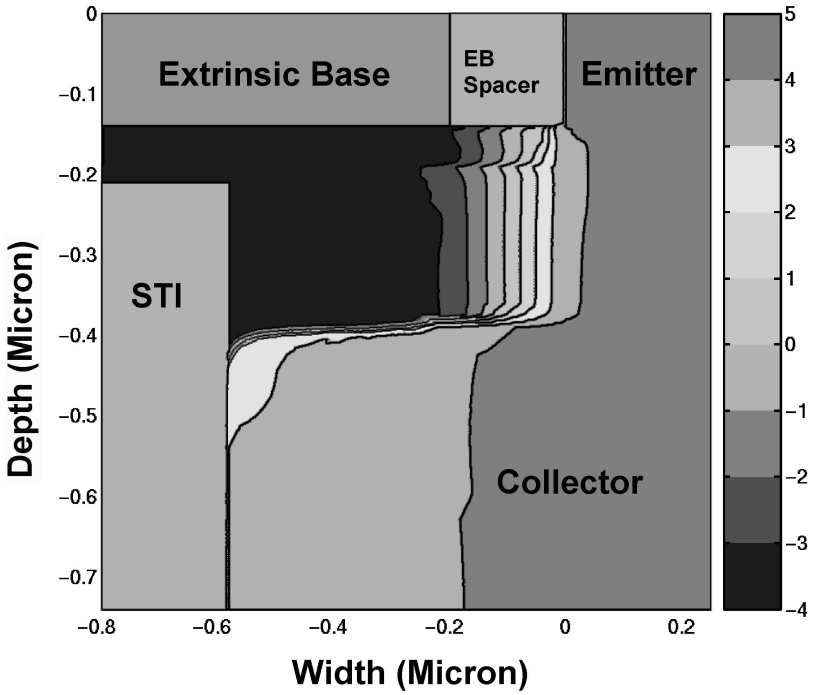

Figure 63: The current contours for 50 GHz SiGe HBTs (5AM) at 85 K.

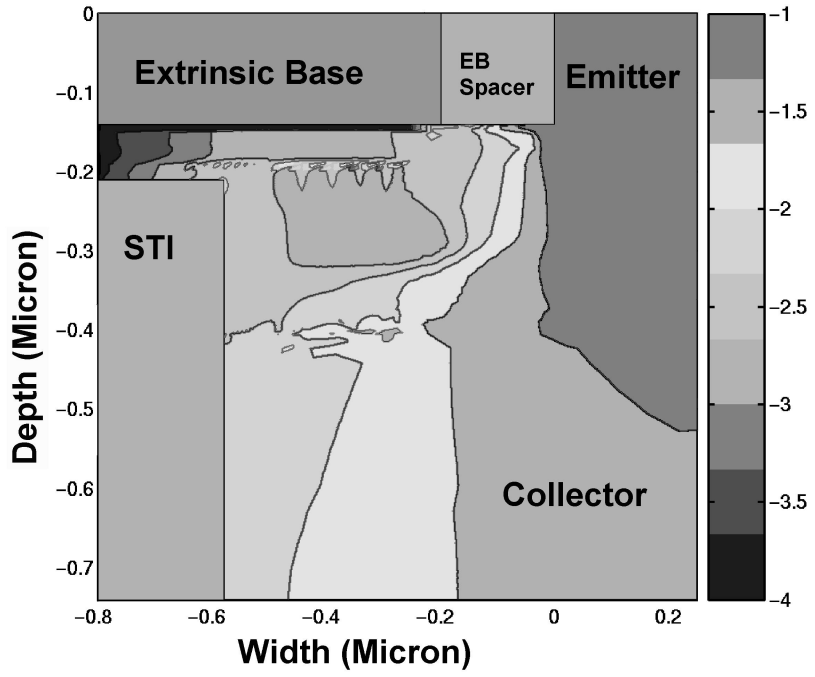

Figure 64: The current contours for inverse mode with $I_C = 1$ nA at 300 K.

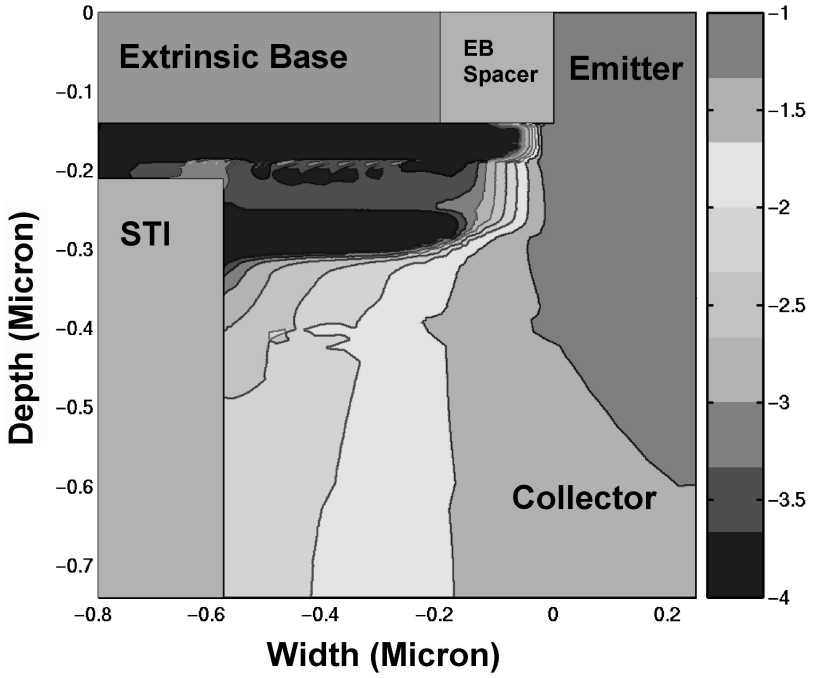

Figure 65: The current contours for inverse mode with $I_C = 1$ nA at 85 K.

4.3.3 Device Lifetime Extraction

Generally speaking, device performance is a function of time since the device parameters tend to change as the operating time accumulates. To guarantee long-time reliability, many device lifetime projection techniques have been developed. For example, one widely adopted method is to generate Arrhenius plots and extrapolate the failure points and thus satisfy a failure criterion from elevated temperatures down to the operating temperature. However, this usually requires a lengthy stress time, which is not easy to realize in a lab environment. Some researchers have therefore used acceleration methods. For example, Neugroschel *et al.* [18] investigated the device lifetime with current-acceleration method in reverse EB stress at room temperature. Rieh *et al.* [20] developed an accelerated current stress technique using high forward current stress to project the device lifetime.

As shown in Chapter 2, MMS can result in considerable damage to the device even within 1000 seconds. Therefore, in this section, the 50 GHz SiGe HBT lifetime projections at room and cryogenic temperatures are introduced based on the MMS method. First, the accelerated stresses were carried out with four different emitter current densities J_E (10 mA/μm^2, 26 mA/μm^2, 28 mA/μm^2,

and 30 mA/μm^2) at a fixed V_{CB} (3 V) and stress temperature (300 K). Figure 66 shows the base current degradation profile at $V_{BE} = 0.7$ V for each stress condition at 300 K. Interestingly, the four

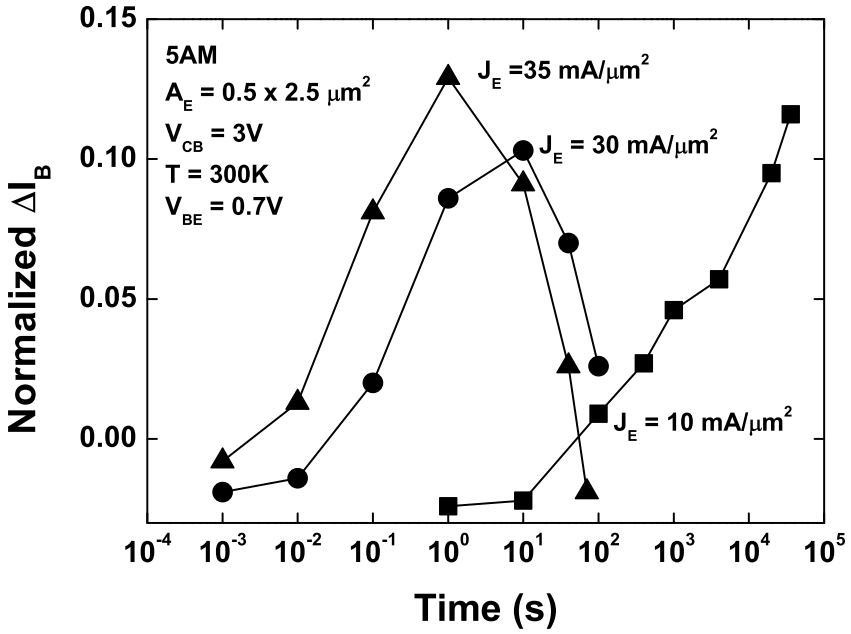

Figure 66: Base current degradation profiles for four emitter stress current densities with fixed V_{CB} (3V) at 300 K.

degradation curves are very similar to each other. With higher stress current density, the degradation rate is faster, and the damage curve shifts toward the direction of time decreasing. When using a 10% I_B change as a criterion, the time for each stress condition can be obtained. At 85 K, a similar trend can be found for three different J_E (26 mA/μm^2, 30 mA/μm^2, and 35 mA/μm^2). Figure 67 shows the base current degradation trend for each stress condition at 85 K. Again, the time to reach the 10% I_B change was recorded. Note that the "projected V_{BE}" is used to keep pre-stress base current constant in order to determine the initial (pre-stress) V_{BE} point at 85 K. In this measurement, the base current at $V_{BE} = 0.7$ V is taken from the pre-stress 300 K Gummel, then this base current is projected to the 85 K pre-stress Gummel to reveal the corresponding V_{BE} (≈ 1.01 V). This V_{BE} is referred to as the "projected V_{BE}". All post-stress base currents at 85 K are based on this V_{BE} point.

Once all the time points that meet the criterion were obtained at both temperatures, Figure 68 was plotted and used to estimate the device lifetime under given current densities. The inferred

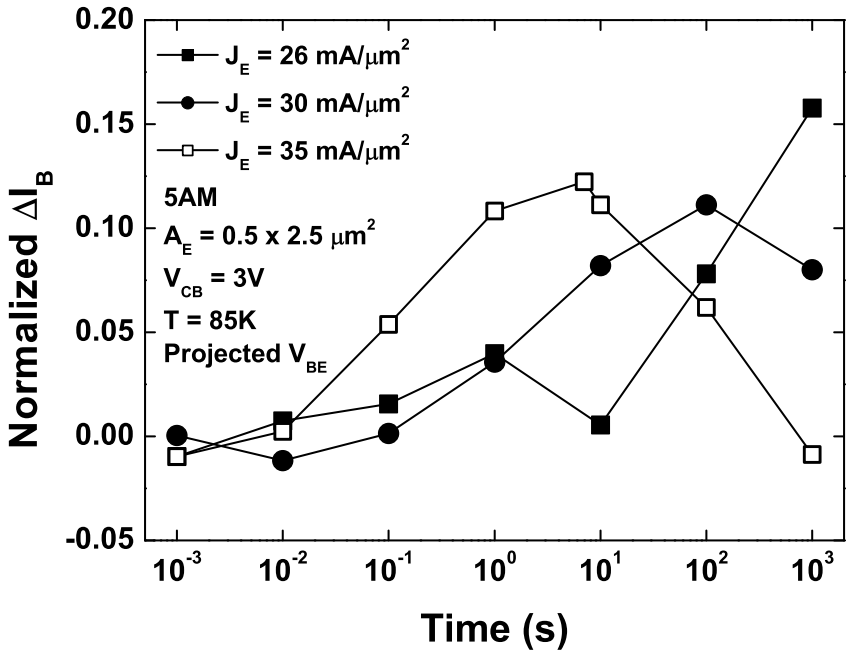

Figure 67: Base current degradation profiles for three emitter stress current densities with fixed V_{CB} (3V) at 85 K.

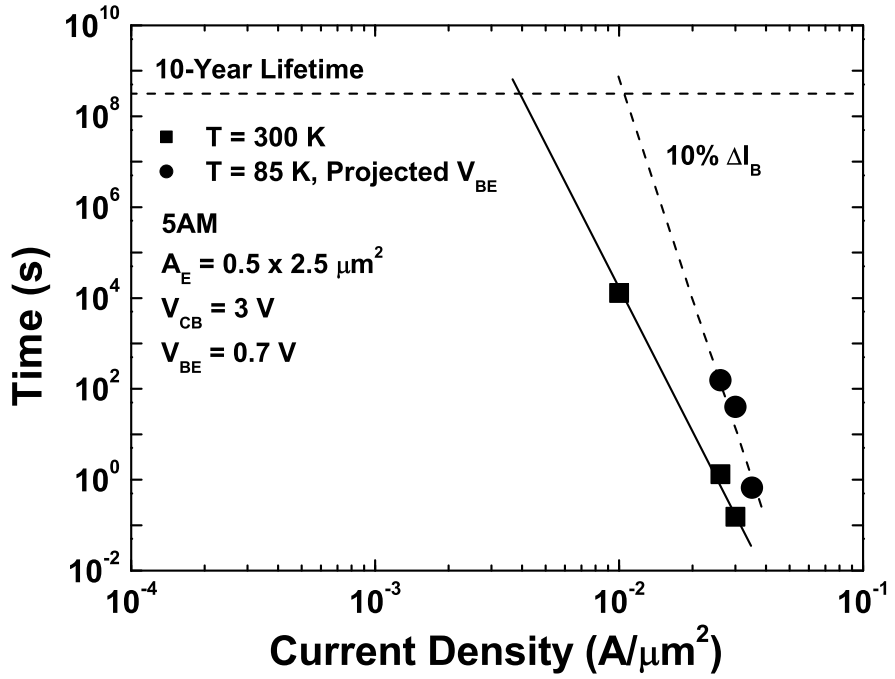

Figure 68: Inferred lifetimes at both 300 K and 85 K by Mixed-Mode Stress.

lifetime τ is clearly longer at cryogenic temperatures, which is consistent with Figure 59. Figure 68 suggests that to satisfy the 10-year lifetime requirement the device has to work under around 4 mA/μm^2 at 300 K with V_{CB} = 3 V, while approximately 10 mA/μm^2 at 85 K with the same V_{CB}. That means that the device can have both better current output driving capability and better reliability at lower temperature at the same time, which is a good news for circuit designers.

As discussed earlier, the base current degradation is caused by the hot carriers generated during MMS. Reverse-EB stress can also generate hot carriers, creating traps at the EB spacer and inducing base current leakage. Figure 69 shows how the inferred lifetime for 50 GHz SiGe HBTs (5AM) is much worse at 85 K than at 300 K using the current-accelerated method [18] where the configuration consists of an open collector and the current is injected into the emitter to bias EB junction reversely. The reliability is worse in cryogenic environments due to the longer mean free path of hot carriers

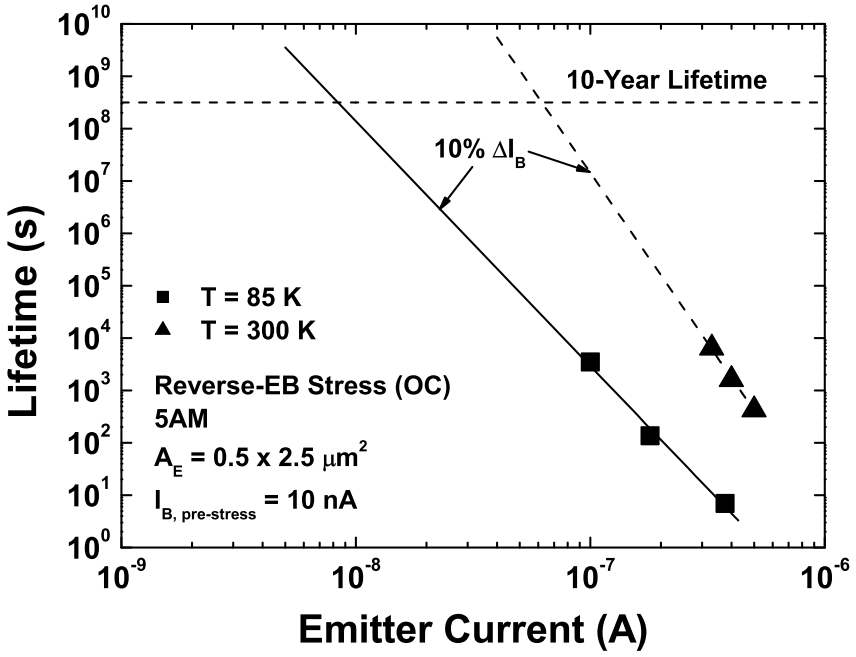

Figure 69: Inferred lifetimes at both 300 K and 85 K by reverse-EB Stress.

at lower temperature. The lifetime extraction results are so different that this again suggests there are different damage mechanisms for MMS and reverse-EB stress.

4.4 Mixed-Mode Stress At High Temperature

Previous sections have shown how SiGe HBTs easily withstand cryogenic temperatures during MMS. This section will focus on MMS reliability at high temperatures. The devices in these tests used IBM 7HP SiGe BiCMOS technology.

Based on the reliability performance of SiGe HBTs at cryogenic temperatures and the current sweep stress results over a range of temperatures, the reliability of SiGe HBTs is expected to be worse at high temperatures. Theoretically, the approach used in Figure 59 can be implemented here again. However, this is not easy for real measurements as at high temperatures, the aluminum pads (emitter, base, and collector contact) melt slightly, making it hard to maintain a good contact. The Gummel curves can't be perfectly overlaid, introducing large measurement errors.

Here, I introduce a model to normalize the degradation ratio from high temperature to room temperature. Assuming that the base current degradation is proportional to the trap density, the base degradation current can be modeled as:

$$\Delta I_B = N_{trap} \times I_s(T) \times (e^{qV_{BE}/nkT} - 1) \tag{23}$$

where N_{trap} is the number of traps and I_s(T) is the recombination saturation current caused by one trap. I_s(T) is a function of ambient temperature, but N_{trap} does not change after stress. The total base current I_B is:

$$I_B = I_{B0} + \Delta I_B \tag{24}$$

where I_{B0} is the base current excluding the current due to stress induced traps. All I_Bs are functions of V_{BE} and temperature T. A variable K can be defined:

$$K = \frac{I_B(x) - I_{B,pre}}{I_B(1000) - I_{B,pre}} = \frac{\Delta I_B(x) - \Delta I_{B,pre}}{\Delta I_B(1000) - \Delta I_{B,pre}} = \frac{N_{trap}(x) - N_{trap,pre}}{N_{trap}(1000) - N_{trap,pre}} \tag{25}$$

where $I_B(x)$, $I_B(1000)$, and $I_{B,pre}$ are the measured base current at stresses lasting x seconds, 1000 seconds, and pre-stress, with fixed V_{BE} and temperature.

During the measurement, $I_{B,pre}$ at room temperature is recorded first. Then the ambient temperature is raised to an assigned high temperature, and $I_{B,pre}$ is read again. After 1000 second stress (I_B is measured at assigned time points), the device is cooled down to room temperature, and $I_{B,post}$

at room temperature is recorded. Assume the trap keeps unchanged in cooling, the K factor can be written as:

$$K = \frac{I_B(x) - I_{B,pre}}{I_B(1000) - I_{B,pre}}\Big|_{high-T} = \frac{I_B(x) - I_{B,pre}}{I_B(1000) - I_{B,pre}}\Big|_{room-T} \tag{26}$$

$I_B(x)$ at room temperature is the only unknown variable. Thus, it can be easily calculated out. Figure 70 shows the results at pre-determined stress time points. The DUTs were stressed over a

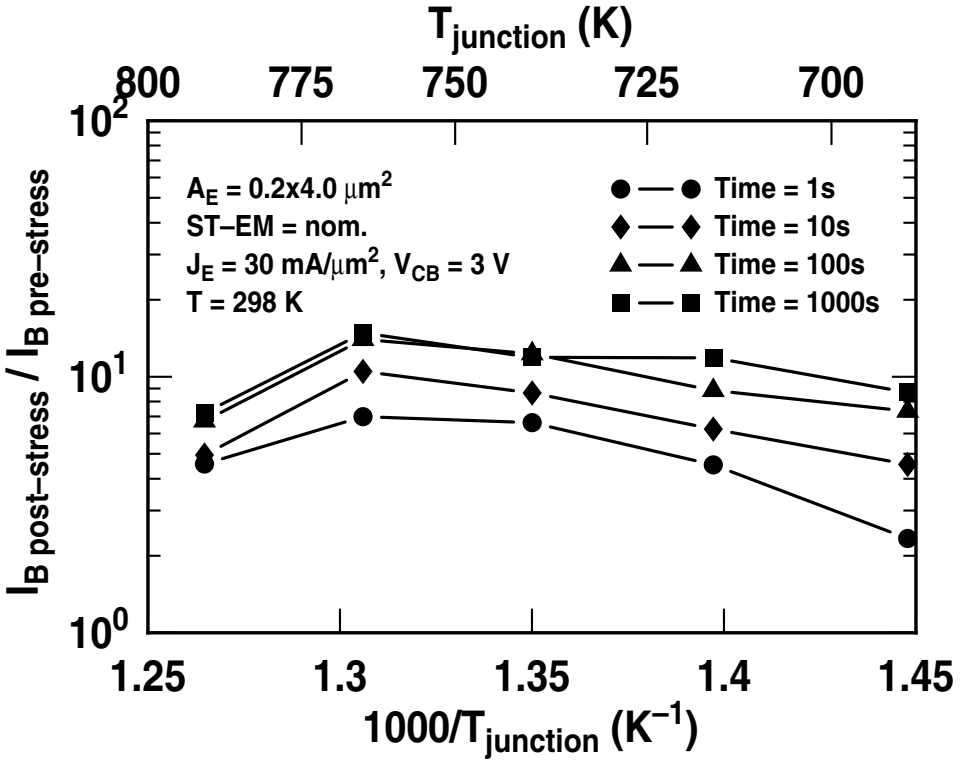

Figure 70: Base current damage ratio vs. $1000/T_{junction}$ at different time points at room temperature.

temperature range of 25 °C to 125 °C by 30 mA/μm^2 + 3.0 V for time cumulative stress technique. Clearly, up to 100 °C (or T_j = 770 K) additional traps were generated with increasing temperature. Again, the results support the conclusion that both impact ionization and self-heating contribute to MMS.

4.5 Summary

In this chapter, reliability issues for 50 GHz SiGe HBTs were examined at cryogenic temperatures (down to the temperature of liquid nitrogen) for emerging mixed-signal cryogenic circuits. Comprehensive mixed-mode reliability stress data for these SiGe HBTs were measured from 300 K and 85 K. The thermal resistances over temperatures were extracted in order to evaluate the impact of the self-heating at low temperatures. The low-frequency noise performance at room temperature and cryogenic temperatures was explored as a function of stress condition. 2D MEDICI simulations were also used to better understand the reliability physics. The inferred lifetime from MMS was compared with that due to reverse-EB stress at 85 K. The results showed opposite trends, indicating that different damage mechanisms were involved. The last section examined MMS at high temperatures with 7HP SiGe HBTs.

CHAPTER V

CONCLUSIONS AND FUTURE WORK

The contributions made by this work can be summarized as follows:

1. A comprehensively Study of the Mixed-Mode Stress (MMS) across multi-generation SiGe HBTs was conducted, including the development of a new time cumulative stress technique. The result revealed the effect of impact ionization for MMS [23][24]. The current sweep stress technique was used to reveal the role of self-heating effect in the MMS [25].

2. The temperature-dependent damage threshold was determined using current sweep stress, after which the P/A and scaling issues for MMS were explained [25].

3. 2D MEDICI simulations using lucky-electron gate current model were implemented successfully for MMS study [23][24][62].

4. After conducting the first assessment of the reliability of SiGe HBTs at extreme temperature environment by the MMS, the inferred lifetime at cryogenic temperatures were extracted for mixed-mode stress, and compared with the lifetime extracted by current-accelerate reverse-EB stress [62].

The two main effects that have been found for MMS suggest a promising series of research studies that can be performed in the future:

1. A study of the hot carrier transport for MMS. In addition to high junction temperature and avalanche breakdown during the MMS, the hot carrier scattering can also be achieved by optical phonons, or even photons. To accomplish the study, special test structures and tests will be needed.

2. A study of the threshold behavior. This research has demonstrated that the damage threshold for the current sweep stress (CSS) has a temperature dependency. However, it is yet to be

determined if Ge profile affects the threshold, and the threshold behavior changed across the device generations.

3. A study of the reliability of the SiGe HBTs at deep cryogenic temperatures (e.g. 43 K) using MMS and other stress techniques (e.g. reverse-EB stress). The study may include a series of measurement splits: (a) with different Ge profiles, (b) different generations.

4. A study of the trap kinetics. The post-stress annealing measurements for MMS and reverse-EB stress reveal the different trap kinetics. Recent data from mixed-mode anneal region also obtained similar results. Thus, further investigation of this behavior is required to understand the trap kinetics.

5. Building a lifetime model. This model should take into account both impact ionization and temperature dependence, and be consistent with CSS results.

6. Simulation of the self-heating effect in MMS. Currently, both the simulators, MEDICI and DESSIS, do not converge when the self-heating option is turned on at ultra high input power. Moreover, Monte-Carlo simulations haven't yet been tried. Therefore, to further probe the damage physics under MMS, MC simulation and simulations with self-heating effect turned on need to be performed.

APPENDIX A

MEDICI CODES

A.1 Mesh Generation

The following MEDICI code was used for the 7HP SiGe HBT mesh generation.

```
TITLE SiGe HBT simulation
COMMENT Grid Generation and Initial Biasing

assign name=y0 n.val=0.1446
assign name=y1 n.val=0.162
assign name=y2 n.val=0.190
assign name=y3 n.val=0.225
assign name=y4 n.val=0.81
assign name=ge1 n.val=0.235 (Ge profile: 23.5%)

COMMENT Specify a rectangular mesh
MESH out.fil=mesh.msh
X.MESH L=-0.8 N=1
x.mesh width=0.8 n.spaces=10 h2=0.03
x.mesh width=0.22 h1=0.03 h2=0.03

y.mesh depth=@y0 h1=0.001 h2=0.001
y.mesh depth=@y1-@y0 n.spaces=20
y.mesh depth=@y2-@y1 n.spaces=30
y.mesh depth=@y3-@y2 n.spaces=30
```

```
y.mesh depth=0.6-@y3 h1=0.0025 h2=0.005
y.mesh depth=0.23 h1=0.005 h2=0.04

eliminate rows x.min=-0.8 x.max=0 y.max=0.14
eliminate rows x.min=-0.8 x.max=0 y.max=0.14
eliminate columns y.min=0.4

COMMENT Region definition
$region NUM=1 silicon y.min=0 y.max=0.1493
$region num=1a silicon y.min=0.1493
region num=1a SiGe y.min=0 y.max=@y1 x.mole=0 x.en=0 y.linear
region num=2 SiGe y.min=@y1 y.max=@y2 x.mole=0 x.end=@ge1 y.linear
region num=3 SiGe y.min=@y2 y.max=@y3 x.mole=@ge1 x.end=0 y.linear
$region num=4 SiGe y.min=@y3 x.mole=@ge1 x.end=@ge1 y.linear
region num=4 silicon y.min=@y3
region num=5 oxide x.max=0 y.max=0.14
region num=6 oxide x.max=-0.3 y.min=@y3

COMMENT Electrodes
ELECTR NAME=Base Y.MIN=0 Y.MAX=0.15 x.max=-0.2
ELECTR NAME=Emitter x.min=0 x.max=0.22 top
ELECTR NAME=Coll BOTTOM

COMMENT Read in impurity profiles from ASCII (SIMS data)
$ dope the whole structure (n-epi)
profile n-type uniform n.peak=1e13

$ extrinsic base to connect the intrinsic base to electrode
profile p-type x.max=-0.1 y.min=0 n.peak=1.5e19 y.max=0.28
```

```
+ x.erfc y.char=0.08 x.char=0.05

COMMENT Read in impurity profiles from ASCII
$ burier doping
profile 1d.ascii in.fil=asm2.dat
+ y.column=1 n.column=2

$ collector doping (lateral extension not real)
profile 1d.ascii in.fil=phosm.dat
+ y.column=1 n.column=2

$ intrinsic base doping
Profile 1d.ascii in.fil=boronm.dat
+ y.column=1 p.column=2

$ emitter doping
Profile 1d.ascii in.fil=asm.dat x.min=0 x.max=0.28 x.erfc x.char=0.015
+ y.column=1 n.column=2

Regrid x.min=-0.08 x.max=0.00 y.min=0.14 y.max=0.2 x.spacin=0.005
Regrid doping ratio=0.5 Logarith x.min=-0.1
save out.file=mdc.msh

stop
```

A.2 Initial Biasing

The code listed below was used to determine the initial biasing conditions. The following sequence is used: sweep V_{BE} to reach the desired current density, then sweep V_{CB} to reach the assigned number. The self-heating option was turned off due to convergency issues.

TITLE 2-D SiGe HBT MMS

COMMENT Initial Biasing

assign name=dirn c.val="./GUMMEL300D/"

assign name=vcb c.val="3"

assign name=temper n.val=300

assign name=sufix c.val="mdc"

assign name=logfile c.val="h-"@sufix

assign name=ie n.val=-30e-3

mesh in.fil=@sufix".msh"

$plot.2d FILL grid (*If want to see the mesh structure*)

$ELECTR NAME=Sink y.min=0.7 Thermal (*If turn on the self-heating, add this electrode*)

$save out.file=mdc.msh

call file=s300.inp (*call model and parameters setup*)

SYMB NEWTON CARRIERS=2 ELE.TEMP HOL.TEMP ∧LAT.TEMP (*Lattice T is not necessary if self-heating is off*)

method damped itlimit=40 stack=10 cont.stk (*modify these methods if meet convergency issue*)

solve v(emitter)=0 v(coll)=0 v(base)=0 (*with self-heating, add T(Sink)=300*)

$ VBE loop

```
assign name=ve n.val= 0
assign name=nstep n.val=31
log out.fil=myfg.log
loop steps=@nstep
solve v(base)=0 v(coll)=0 v(emitter)=-@ve
assign name=ve n.val=@ve+0.05
l.end

solve v(base)=0 v(coll)=0 v(emitter)=-1.5

$ current BC
CONTACT name="emitter" Current
solve v(base)=0 v(coll)=0 i(emitter)=@ie

$ VCB loop
assign name=vcb n.val= 0
assign name=nstep n.val=61
loop steps=@nstep
solve v(base)=0 v(coll)=@vcb i(emitter)=@ie
assign name=vcb n.val=@vcb+0.05
l.end

COMMENT output Gummel
plot.1d x.ax=v(emitter) y.ax=I(coll) y.log out.fil=@dirn"fg-IC-T"@temper"K.txt"
+ device=cl/postscript plot.out=tmp.ps

plot.1d x.ax=v(emitter) y.ax=I(base) y.log out.fil=@dirn"fg-IB-T"@temper"K.txt"
+ device=cl/postscript plot.out=tmp.ps
```

save out.file=@dirn"stress-"@sufix"-T"@temper"K.tif" all tif

The following codes are for impact ionization simulation setup (models and parameters).

COMMENT s300.inp

MODELS bgn phumob CONSRH AUGER ∧TMPMOB ∧EF.TMP ∧ET.MODEL temp=@temper

+ impact.i ii.nloc=0 (*non-local impact ionization*)

+ gate2=true gate.gen=1 gate.sur=false (*gate current analysis module*)

assign name=v0 n.val=6.92e-3

assign name=v0sg n.val=4e-3

assign name=n0 n.val=1.3e17

assign name=n0sg n.val=2e19

assign name=con n.val=0.5

assign name=consg n.val=0.0

material nsrhn=1e17 nsrhp=1e17 polysili

material nsrhn=1e17 nsrhp=1e17 silicon

material nsrhn=1e17 nsrhp=1e19 sige

assign name=scale n.val=1 (*scale factor*)

material polysilicon taun0=@scale*30e-6 taup0=@scale*10e-6

material silicon taun0=@scale*30e-6 taup0=@scale*10e-6

material sige taun0=@scale*30e-6 taup0=@scale*10e-6

material silicon v0.bgn=@v0 n0.bgn=@n0 con.bgn=@con

material sige v0.bgn=@v0sg n0.bgn=@n0sg con.bgn=@con

material polysili v0.bgn=@v0 n0.bgn=@n0 con.bgn=@con

A.3 Hot Carriers Calculation

The codes listed below were used for the hot electron calculation. Since MEDICI can't converge for two oxides at the same time, the gate current analysis must be performed sequentially. It is preferable for convergency reasons to calculate the STI oxide first, followed by the EB spacer.

```
COMMENT Show Hot Electrons
assign name=dirn c.val="./GUMMEL300D/"
assign name=vcb c.val="3"
assign name=temper c.val="300"
assign name=mname c.val="mdc"

mesh in.file=@mname".msh"
load in.file=@dirn"stress-"@mname"-T"@temper"K.tif" tif (load in initial biasing result)

MODELS bgn phumob CONSRH AUGER ^TMPDIFF ^TMPMOB ^EF.TMP ^ET.MODEL
+ impact.i ii.nloc=0 ii.temp gate2=true gate.gen=1 gate.sur=false gate.tem=true

assign name=v0 n.val=6.92e-3
assign name=v0sg n.val=4e-3
assign name=n0 n.val=1.3e17
assign name=n0sg n.val=2e19
assign name=con n.val=0.5
assign name=consg n.val=0.0

material nsrhn=1e17 nsrhp=1e17 polysili
material nsrhn=1e17 nsrhp=1e17 silicon
material nsrhn=1e17 nsrhp=1e19 sige
```

```
assign name=scale n.val=1
material polysilicon taun0=@scale*30e-6 taup0=@scale*10e-6
material silicon taun0=@scale*30e-6 taup0=@scale*10e-6 lamhn=9.7e-7 (lamhn: hot electron scattering mean free path in Si)
material sige taun0=@scale*30e-6 taup0=@scale*10e-6 lamhn=9.7e-7 (lamhn in SiGe is same as in Si)
material silicon v0.bgn=@v0 n0.bgn=@n0 con.bgn=@con
material sige v0.bgn=@v0 n0.bgn=@n0 con.bgn=@con
material polysili v0.bgn=@v0 n0.bgn=@n0 con.bgn=@con

$ reg: oxide1 mat: oxide is the STI oxide
$ reg: oxide2 mat: insulato is the EB spacer

$ ONLY STI

material oxide eg300=4.00 affinity=2.40 (STI activation energy)

symbolic newton carriers=2 ele.temp hol.temp ^lat.temp
method damped n.maxbl=40 itlimit=40 stack=10 cont.stk
solve impact.ii gate.cur

save out.file=@dirn"s5hp-"@mname"-sti-T"@temper"K.tif" all tif

plot.3d g.gamt x.min=-0.1 x.max=0.1 y.min=0 y.max=0.8
+ device=cl/postscript plot.out=@dirn"gam-sti.ps"
plot.3d g.it x.min=-0.1 x.max=0.1 y.min=0 y.max=0.8
extract name="g.gamt" expressi="g.gamt" x.min=-0.1 x.max=0.1 y.min=0 y.max=0.4
```

```
COMMENT ONLY EB spacer

mesh in.file=@mname".msh"
load in.file=@dirn"stress-"@mname"-T"@temper"K.tif" tif

MODELS bgn phumob CONSRH AUGER ^TMPDIFF ^TMPMOB ^EF.TMP ^ET.MODEL
+ impact.i ii.nloc=0 ii.temp gate2=true gate.gen=1 gate.sur=false gate.tem=true

assign name=v0 n.val=6.92e-3
assign name=v0sg n.val=4e-3
assign name=n0 n.val=1.3e17
assign name=n0sg n.val=2e19
assign name=con n.val=0.5
assign name=consg n.val=0.0

material nsrhn=1e17 nsrhp=1e17 polysili
material nsrhn=1e17 nsrhp=1e17 silicon
material nsrhn=1e17 nsrhp=1e19 sige

assign name=scale n.val=1
material polysilicon taun0=@scale*30e-6 taup0=@scale*10e-6
material silicon taun0=@scale*30e-6 taup0=@scale*10e-6 lamhn=9.7e-7
material sige taun0=@scale*30e-6 taup0=@scale*10e-6 lamhn=9.7e-7
material silicon v0.bgn=@v0 n0.bgn=@n0 con.bgn=@con
material sige v0.bgn=@v0 n0.bgn=@n0 con.bgn=@con
material polysili v0.bgn=@v0 n0.bgn=@n0 con.bgn=@con

material insulato eg300=4.00 affinity=2.40 (EB spacer activation energy)
+ ecn.gc=0 ecp.gc=0
```

```
symbolic newton carriers=2 ele.temp hol.temp ^lat.temp
method damped n.maxbl=40
solve impact.ii gate.cur

plot.3d g.gamt x.min=-0.4 x.max=0.1 y.min=0 y.max=0.8
+ device=cl/postscript plot.out=@dirn"gam-tre.ps"
plot.3d g.it x.min=-0.4 x.max=0.1 y.min=0 y.max=0.8
+ device=cl/postscript plot.out=git-tre.ps

save out.file=@dirn"s5hp-"@mname"-tre-T"@temper"K.tif" all tif
```

Following codes are for some typical output results.

```
COMMENT breakdown
plot.2d BOUND JUNC X.MIN=-0.8 TITLE="5% II GEN" FILL SCALE
+ device=cl/postscript plot.out=@dirn"iigen2d.ps"
CONTOUR II.GENER NCONT=21 COLOR=1

COMMENT current flow
plot.2d BOUND JUNC X.MIN=-0.8 TITLE="5% Flowlines (ii)" FILL SCALE
+ device=cl/postscript plot.out=@dirn"flowlines.ps"
CONTOUR FLOWLINES NCONT=21 COLOR=1

COMMENT POTENTIAL DISTRIBUTION
plot.2d BOUND JUNC X.MIN=-0.8 X.MAX=0.2 Y.MIN=0 Y.MAX=0.8 TITLE="5% Potential"
FILL SCALE
+ device=cl/postscript plot.out=@dirn"potential2D.ps"
```

```
CONTOUR POTENTIA NCONT=21 COLOR=1

COMMENT E FIELD
plot.1d J.EFIELD Y.START=0 Y.END=0.8 X.START=-0.1 X.END=-0.1 out.fil="jE-vertical-cut.txt"
+ device=cl/postscript plot.out=@dirn"jE-vertical-cut.ps"

plot.2d BOUND JUNC X.MIN=-.8 TITLE="5% E FIELD" FILL SCALE
+ device=cl/postscript plot.out=@dirn"jefield2d.ps"
CONTOUR J.EFIELD NCONT=21 COLOR=1

plot.3d J.EFIELD TITLE="ELECTRIC FIELD MAGNITUDE"
+ device=cl/postscript plot.out=@dirn"efield3d.ps"

COMMENT Lattice T
plot.2d BOUND JUNC X.MIN=-0.8 TITLE="5% LATTICE TEMPERATURE" FILL SCALE
+ device=cl/postscript plot.out=@dirn"latticeT.ps"
CONTOUR LAT.TEMP NCONT=21 COLOR=1
```

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